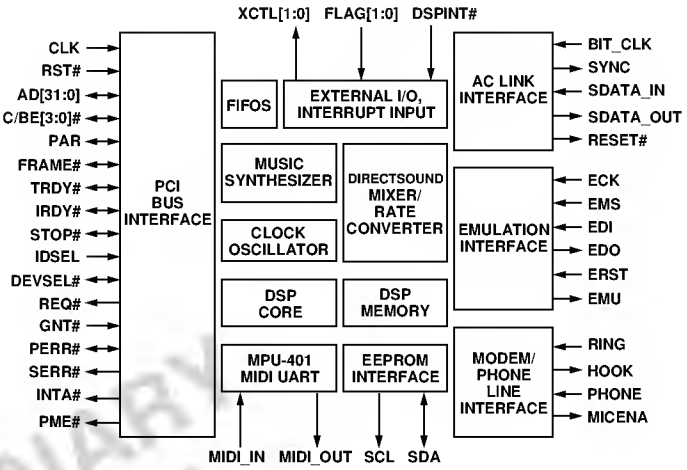
PCI SoundComm® DC '97 Digital Controller

AD1818

FEATURES

- Single-Chip 5 V PCI Digital Controller for Audio and Communications Acceleration Applications
- 64-Stream DirectSound® Hardware Mixer with Hardware Rate Conversion
- Supports Full Duplex Capture and Playback Operation at Different Sample Rates
- Supports Multiple Sample Rates Simultaneously
- Sample Rates from 1 Hz to 48 kHz
- Windows® 98 WDM® Drivers Provided with the AD1818
- "Digital Ready" PCI Bus Redirection Supports USB and IEEE 1394 Audio Peripherals
- Integrated Large Memory 66 MIPS ADSP-21csp11 DSP Core Supports:
  - 64-Voice Downloadable Sounds Wavetable Synthesizer
  - 3D Sound Localization
  - 5.1 Channel Dolby Digital® AC-3 Decompression with Virtual Home Theater Processing
  - Telephony Applications
    - V.34 and 56 kbps Voice Modem
    - V.17 Fax
    - V.70 DSVD
    - V.80 Video Conferencing Support
    - Full Duplex Speakerphone with Acoustic Echo Cancellation
    - G.72x Voice Codecs
- Serial Interface to Audio Codec '97 (AC '97)
- Support for Up to Four ADCs and Six DACs on the AC Link Serial Bus
- PCI Bus Master/Target Interface with Scatter-Gather DMA Capability
- On-Chip OPL3® Compatible Music Synthesizer
- MPU-401®-Compatible MIDI UART
- Advanced Power Management Modes and PME# Signal Support ACPI, PCM-PM and On Now®
- 128-Terminal PQFP Package
- Complete Set of Development Tools Available Including ICE, C Compiler, Assembler and Debugger

FUNCTIONAL BLOCK DIAGRAM



INTRODUCTION

The AD1818 5 V PCI SoundComm DC '97 Digital Controller is a full-featured DirectSound and telephony accelerator. In addition to processing DirectSound3D® coefficients locally, the AD1818 supports a 64-voice downloadable sounds wavetable engine, a music synthesizer, a 33.6 kbps V.34/56 kbps V.PCM voice modem data pump/controller (with 14400 bps fax) and a Dolby Digital AC-3 decoder. The AD1818 provides an integrated audio and telephony solution for Windows 98 DirectSound 5.0 audio/TAPI® telephony multimedia applications.

REV. 0

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ORDERING GUIDE

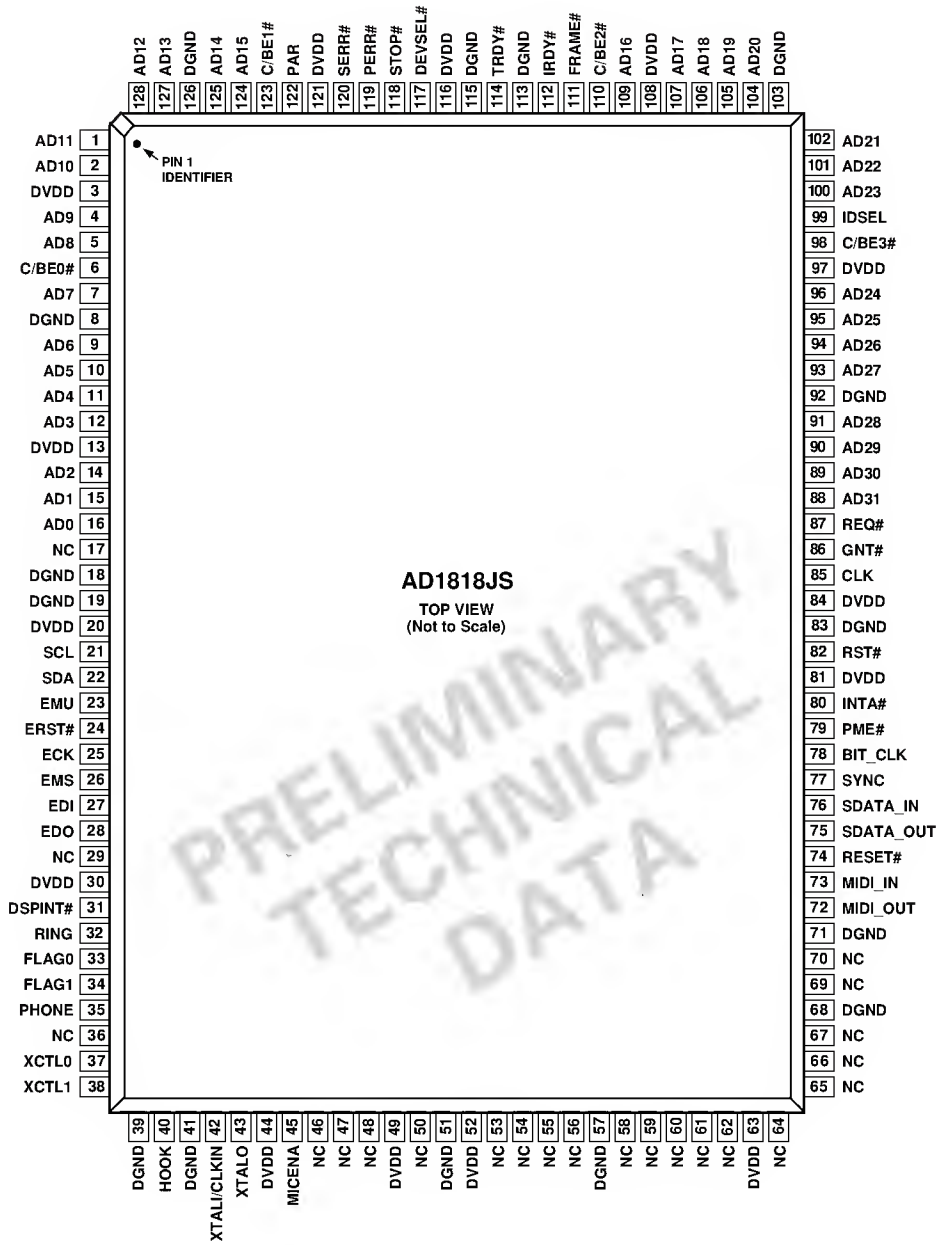
Model	Temperature Range	Package Description	Package Option*
AD1818JS	0°C to +70°C	128-Terminal PQFP	S-128A

*S = Plastic Quad Flatpack.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1818 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

PCI Bus Interface

Pin Name	PQFP	I/O	Description
CLK	85	I	Clock
RST#	82	I	Reset
AD[31:0]	88, 89, 90, 91, 93, 94, 95, 96, 100, 101, 102, 104, 105, 106, 107, 109, 124, 125, 127, 128, 1, 2, 4, 5, 7, 9, 10, 11, 12, 14, 15, 16	I/O	Address/Data Bus
C/BE[3:0]#	98, 110, 123, 6	I/O	Command/Byte Enables
PAR	122	I/O	Parity
FRAME#	111	I/O	Cycle Frame
TRDY#	114	I/O	Target Ready
IRDY#	112	I/O	Initiator (Master) Ready
STOP#	118	I/O	Stop
IDSEL	99	I	Initialization Device Select
DEVSEL#	117	I/O	Device Select
REQ#	87	O	Request
GNT#	86	I	Grant
PERR#	119	I/O	Parity Error
SERR#	120	O	System Error
INTA#	80	O	Interrupt A
PME#	79	O	Power Management Event. Signal Changes in Power Management State. Requested by AD1818, e.g., Modem Wake-Up On Ring.

AC Link

Pin Name	PQFP	I/O	Description
BIT_CLK	78	I	Serial Clock
SYNC	77	O	Frame Sync
SDATA_IN	76	I	Serial Data Out
SDATA_OUT	75	O	Serial Data In
RESET#	74	O	AC '97 Reset

MIDI Interface

Pin Name	PQFP	I/O	Description
MIDI_IN	73	I	RxD MIDI Input
MIDI_OUT	72	O	TxD MIDI Output

Emulation Interface

Pin Name	PQFP	I/O	Description
ECK	25	I	Emulator Clock
EMS	26	I	Emulator Mode Select
EDI	27	I	Emulator Data Input
EDO	28	O	Emulator Data Output
ERST#	24	I	Emulator Logic Reset
EMU	23	O	Emulator Event Pin

EEPROM Interface

Pin Name	PQFP	I/O	Description
SCL	21	O	Serial Clock
SDA	22	I/O	Serial Data

Modem/Phone Line Interface

Pin Name	PQFP	I/O	Description
RING	32	I	Ring Indicator from DAA
HOOK	40	O	On/Off Hook Control to DAA
PHONE	35	I	Phone Pickup Indicator from DAA
MICENA	45	O	Microphone/Line Source Select

Miscellaneous

Pin Name	PQFP	I/O	Description
XCTL[1:0]	38, 37	O	External Controls
FLAG[1:0]	34, 33	I	Input Flags
DSPINT#	31	I	DSP Interrupt

Crystal/Clock

Pin Name	PQFP	I/O	Description
XTALI/CLKIN	42	I	33 MHz Crystal Input/Clock Input
XTALO	43	O	33 MHz Crystal Output

Power Supplies/No Connects

Pin Name	PQFP	I/O	Description
DGND	8, 18, 19, 39, 41, 51, 57, 68, 71, 83, 92, 103, 113, 115, 126	I	Digital Ground
DVDD	3, 13, 20, 30, 44, 49, 52, 63, 81, 84, 97, 108, 116, 121	I	+5 V Digital Supply Voltage
NC	17, 29, 36, 46, 47, 48, 50, 53, 54, 55, 56, 58, 59, 60, 61, 62, 64, 65, 66, 67, 69, 70		No Connect. Do Not Connect.

ARCHITECTURAL OVERVIEW

Figure 1 shows the functional blocks that make up the AD1818. The AD1818's design is focused to accelerate DirectSound and telephony algorithms. The PCI bus master/bus target interface provides the path for moving DirectSound data from host memory into the AD1818 for further acceleration. The 64-stream digital mixer and sample rate converters, combined with the internal DSP, accelerate mixing, sample rate conversion and 3D localization in hardware. The DSP may also be used to execute wavetable algorithms and Dolby Digital AC-3 decoding functions, and as a telephony data pump/controller. Figure 2 shows a detailed view of the AD1818 internal structure.

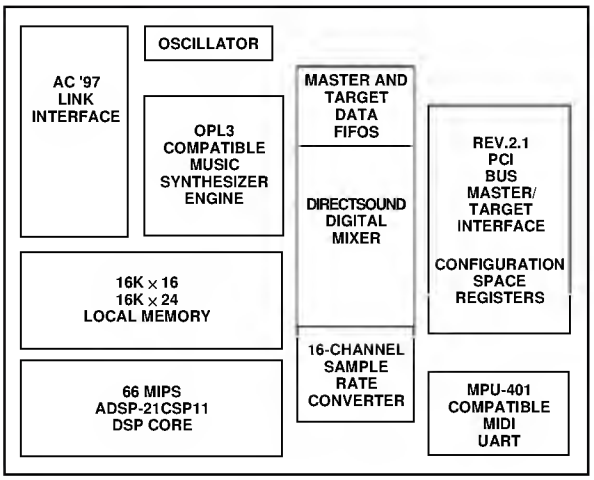


Figure 1. Block Diagram

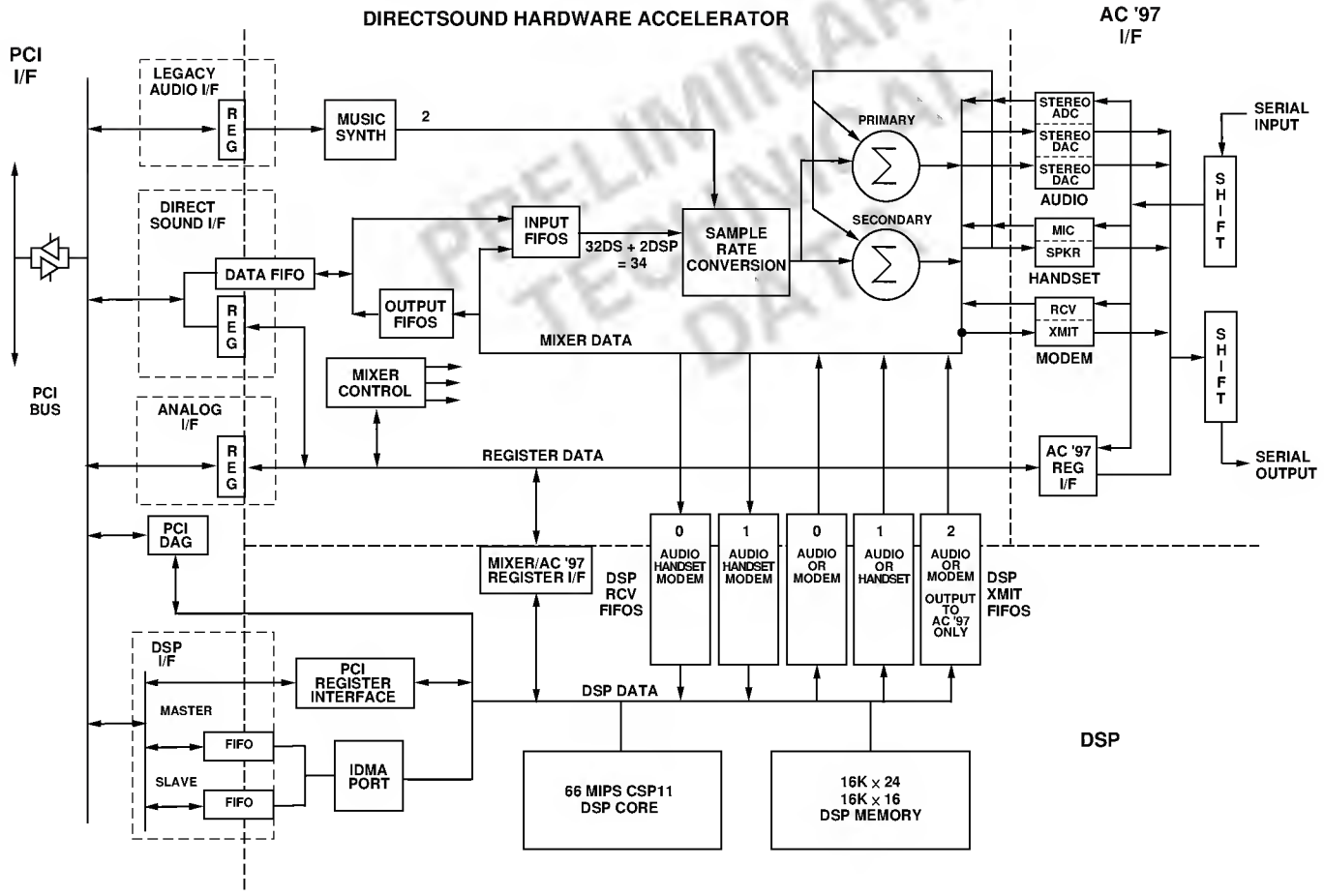


Figure 2. Detailed Block Diagram

INTEGRATING THE AD1818 INTO A TARGET SYSTEM

The system block diagram shows the essential features of an AD1818 design. The AD1818 acts as a master to the AC '97 audio codec providing digital processing for DirectSound audio data as well as communications data streams.

The AC '97 industry standard codec interface provides a direct connection point for an AC '97 compatible codec such as the AD1819 from Analog Devices.

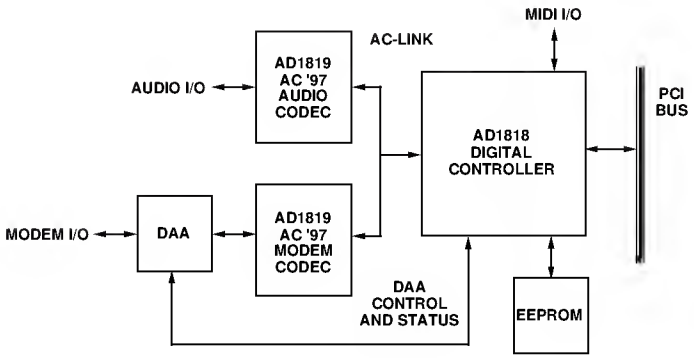


Figure 3. System Block Diagram

SOFTWARE DRIVER SUPPORT

The AD1818 Windows 98 DirectSound WDM drivers play a critical role in arbitrating AD1818 and system resources. Any algorithm or acceleration function such as digital mixing may be locally processed on the AD1818, the host or a combination of both.

A real-time operating system kernel runs on the DSP and performs several functions. These include:

- Algorithm Loading
- Algorithm Initialization
- Algorithm Execution
- Algorithm Termination
- AD1818 Resource Sharing (Algorithm Cooperation)
- Real-Time Task Scheduling and Execution Preemption
- Clock and Timer Functions

AUDIO SOURCES

DirectSound

The AD1818 contains a 64-stream digital mixer block for DirectSound buffers. Four output channels are produced from the mixer, two of which are the primary audio left and right outputs. Each of the four channels can be optionally transferred back to the host for further processing.

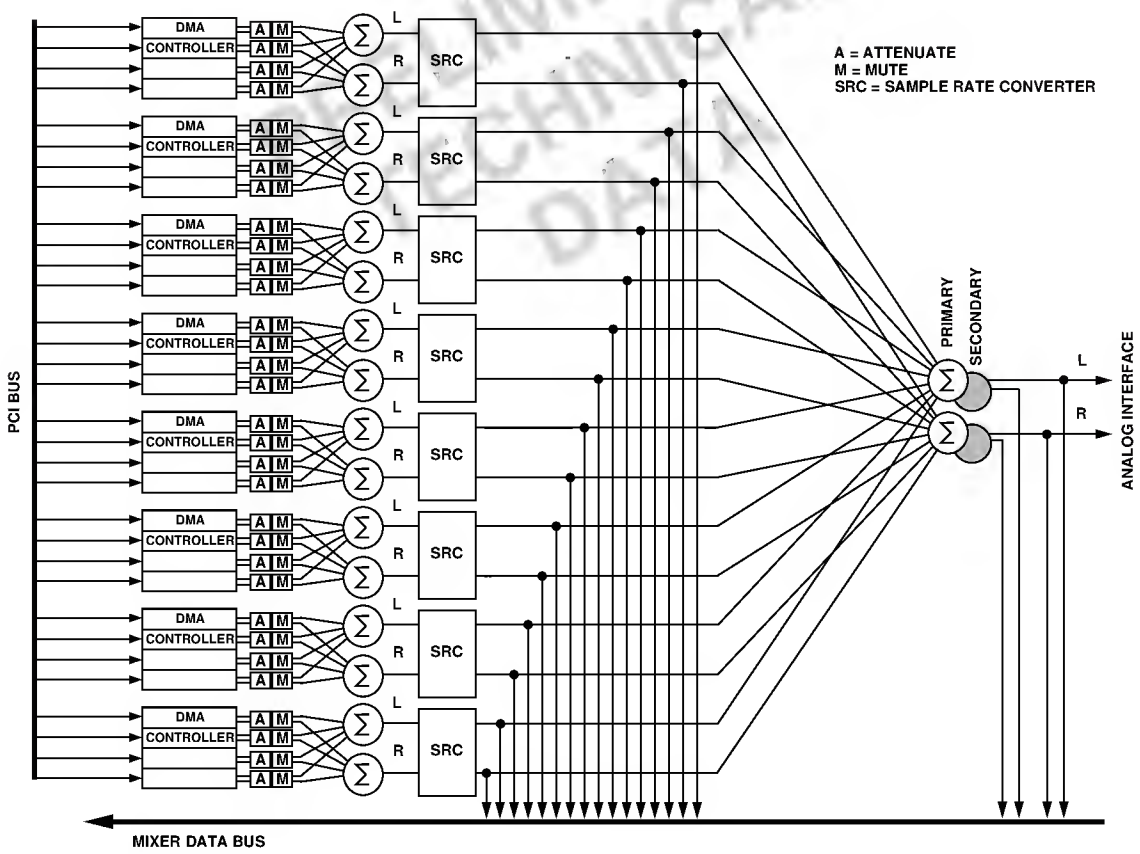


Figure 4. Basic DirectSound Digital Mixer and Sample Rate Converters

DirectSound Mixer

One of the principal features of DirectSound is mixing. Most games open between three to eight sound buffers and mix them simultaneously. A buffer contains either a mono or a stereo source. When multiple sounds are mixed in software, CPU utilization increases and system latency may cause sounds and visual cues to become unsynchronized. In order to allow games to run faster and more smoothly, the AD1818 has a built-in hardware mixer capable of mixing and sample rate converting up to 64 digital streams. The stereo output of the mixer may be sent the analog interface, the DSP for digital processing as in DirectSound 3D and effects, or returned to the host via the PCI Bus.

The AD1818's 32-channel PCI DMA Controller interface transfers either 32 stereo channels (64 streams) or 32 mono streams into the hardware mixer. The DMA controller directs the playing or stopping of a sample buffer and is capable of automatically looping to the start of a buffer. The DMA controller counts the number of bytes transferred and can stop playing a sample after a specified number of bytes have been transferred. If the number of bytes is greater than the length of the buffer, the buffer automatically loops back to the beginning.

After initiating a DMA transfer, the sample data enters the AD1818 mixer. Attenuation blocks (A) control the volume of a sample from 0 dB to –94.5 dB in 1.5 dB steps for the left and right channel of each stream, or the stream can be completely muted (M). Panning is supported by a combination of the left and right attenuation blocks, making the sound move across a sound field.

The streams are then summed together in blocks of four. Every four streams of left channel data (must be at the same sample rate) are summed together as well as every four streams of right channel data (same sample rate) producing eight separate samples of left and right data. The eight stereo samples then enter the sample rate converter block (SRC). Eight independent programmable SRC blocks convert the summed samples from a user-specified sample rate to the AC '97 standard sample rate of 48 kHz. The input sample rate ranges from 1 Hz to 48 kHz in 1 Hz increments. The resulting left data may be returned to the Mixer Data Bus or summed to produce one left output stream. Right digital data may be returned to the Mixer Data Bus or summed to produce one right output stream completing the stereo sample pair of the Primary Summer. The stereo output of the Primary Summer may be sent to either the Mixer Data Bus or the Analog Interface. The Secondary Summer provides an additional stereo output for the Mixer Data Bus, which may be sent to the DSP for effects processing or routed back to the PCI bus.

Extended DirectSound Mixer

In addition to the AD1818's Basic DirectSound Mixer, an Extended Mixer and SRC stage handles streams sent to the Mixer Data Bus from the DSP and the internal Music Synthesizer.

The Extended Mixer allows for further processing and remixing of data. For example, data handled by the Basic Mixer may be sent to the DSP for effects processing and then mixed with the AD1818's output to generate effects such as echo and reverberation or DirectSound3D.

Sample Rate Converter

The sample rate converter (SRC) blocks attached to the basic and extended DirectSound audio streams are variable interpolating SRCs. Each converter accepts samples at the rate of 1 Hz to 48 kHz and interpolates the samples to a common rate of 48 kHz. In addition, a variable decimation SRC is included to accept a single stereo channel of audio data at 48 kHz and decimate the sample to any rate between 1 Hz and 48 kHz.

Utilizing Analog Devices' variable sample rate technology, each SRC employs a scalable anti-aliasing or anti-imaging filter to properly filter the rate converted data. The result is a high performance multiple format and multiple sample rate mixer.

Given the high resolution of the SRCs, the mixer can be used to accelerate the pitch shifting operation for digital effect or music

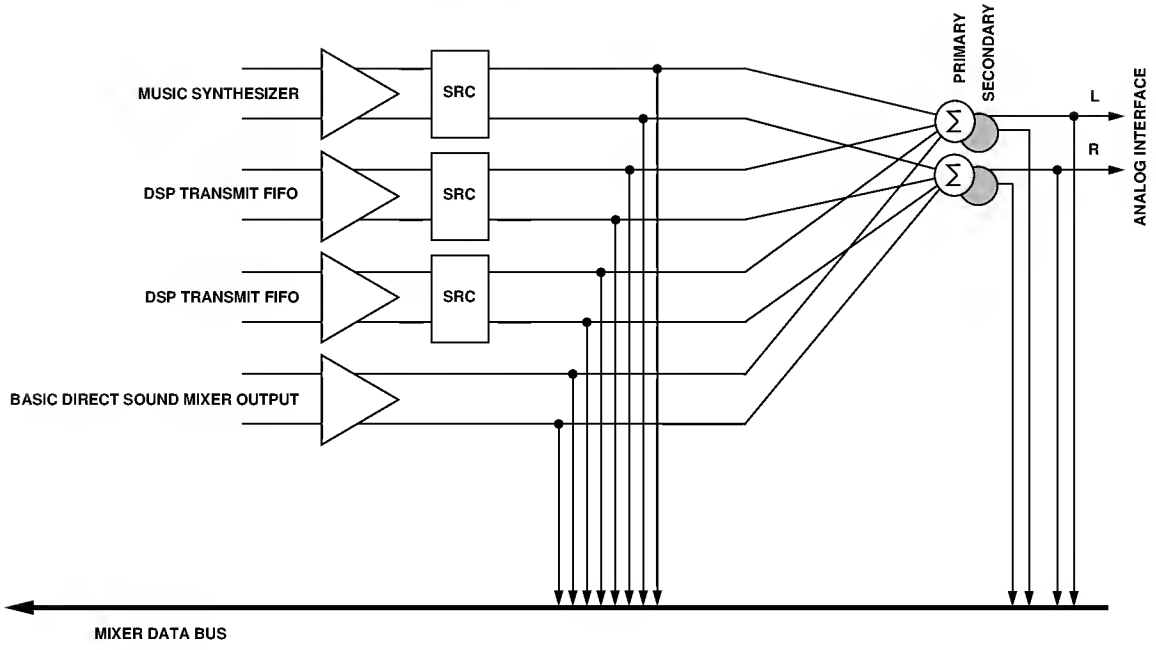


Figure 5. Extended DirectSound Digital Mixer and Sample Rate Converters

generation. Since the interpolated data has a –90 dB SNR performance, the pitch shifting performed by the SRCs has no audible artifacts common in a lower quality pitch shifting algorithms. To shift the pitch, simply program the sample rate register of an audio stream to a different value. For example, to double the pitch of an 8 kHz prerecorded audio sample, program the sample rate register to 16000. Note that the valid range of the frequency register is 1 Hz to 48000 Hz. Sampled data cannot be pitch shifted beyond 48 kHz.

The variable decimation SRC provides a means to reduce audio data storage size by reducing the sample rate cleanly. For example, a 10 second recording of stereo audio data can be acquired at the AC Link as a 1.92 Mbyte file, or resampled and reformatted in real time with the SRC to a 80 kbyte mono, µlaw compressed, 8 kHz file.

MUSIC SYNTHESIS

The AD1818 includes an embedded music synthesizer that emulates industry standard OPL3 FM synthesizer chips and delivers 20-voice polyphony. The internal synthesizer generates digital music data at 22.05 kHz. The Music Synthesizer's output is summed with the output stream. The Music Synthesizer on the AD1818 has register readback capability to facilitate power-down save and restore.

The music synthesizer has been developed by Euphonics, a research and development company that specializes in audio processing and electronic music synthesis.

MPU-401-COMPATIBLE MIDI UART

The primary interface for communicating MIDI data to and from the host PC is the hardware MPU-401 compatible interface. The MPU-401 compatible interface includes a built-in FIFO for communicating to the host bus.

External EEPROM

Pins SCL and SDA on the AD1818 are available to provide an interface to a serial EEPROM. When a serial EEPROM is connected to the AD1818, the Subsystem Vendor ID and Subsystem Device ID configuration space registers are loaded from the EEPROM. Loading of these registers occurs when the part exits reset. The four bytes are read starting at byte address 0, with the upper byte of the Subsystem Device ID read first followed by the lower byte of the Subsystem Device ID, upper byte of the Subsystem Vendor ID and, lastly, the lower byte of the Subsytem Vendor ID.

The 2-wire interface requires serial EEPROMs such as the X24C01 from Xicor. For the interface to be activated, external pullups are required on the SCL and SDA pins. If the SCL pin is pulled low upon reset, then the interface is automatically disabled and the default values remain in the Subsystem Vendor ID and Subsystem Device ID registers.

DSP SECTION

The DSP in the AD1818 is based on the Analog Devices ADSP-21csp11 processor. Please refer to the ADSP-21csp11 Concurrent Signal Processor data sheet (Analog Devices publication C2180-8-10/96) for additional information on the ADSP-21csp11 core, memory and peripheral features and functions. This 16-bit DSP is optimized for concurrent signal processing and other high speed numeric processing applications. It combines high performance, high bandwidth, 32K words of on-chip memory and fast task switching support to provide efficient multisignal or multichannel processing.

The DSP base architecture consists of computational units, data address generators, a program sequencer and an instruction cache. The DSP on the AD1818 also has a programmable timer, extensive interrupt capabilities and 32K words of on-chip memory. The memory is organized into a single, unified memory space containing two memory blocks with 16K locations in each block. One block is 16K × 24 bits and can be used to store instructions or data, while the other is 16K × 16 bits and can be used to store data.

Additions to the DSP for the AD1818 include a high speed DMA interface to the PCI bus. As a PCI target, the DSP exposes its on-chip memory to the bus, allowing burst transfers via a FIFO to or from the DSP memory. As a bus master, the PCI interface can transfer DMA data between system memory and the DSP. The control registers for these transfers are available both to the host (in PCI memory space) and to the DSP.

Five FIFOs have also been added to interface the DSP to the audio and telephony data streams on the AD1818. The two receive and three transmit FIFOs are each eight words deep and 16 bits wide. Each FIFO has independent control, allowing a DSP interrupt to be generated when any number of words have been added to or taken from the FIFOs. Optionally, the on-chip DMA engine can be programmed to automatically transfer data between the FIFOs and DSP memory.

The DSP also has access to various control registers within the mixer and the analog interface.

The on-chip DSP operates at 66 MHz with a 16 ns instruction cycle time. With its large memory and on-chip instruction cache, the processor can execute most instructions in a single cycle.

The DSP's flexible architecture and comprehensive instruction set supports a high degree of parallelism. In one cycle the DSP can execute all of the following operations:

Perform a Computation
Perform One or Two Data Moves
Update One or Two Data Address Pointers
Generate a Program Address
Fetch an Instruction
Decode an Instruction

The operations take place while the processor continues to complete the following tasks:

Receive and Transmit Data through One or More of the FIFOs
Receive or Transmit Data from the PCI Bus
Decrement the Timer

DSP Boot

Following power-up, the DSP core is held in idle, waiting to be booted. Boot code is downloaded from the PCI bus; there is no other method of booting the AD1818's DSP. During the boot code download process, the host is the PCI bus master and the AD1818 is a slave target. The DSP memory is mapped to PCI address space. This mapping is controlled through Base Address Register 4 in AD1818 PCI configuration space. This register controls the mapping of the on-chip 16K × 24 DSP memory, which is nominally used for program memory. There is a separate register (Base Address Register 5 in AD1818 PCI configuration space) that maps the on-chip 16K × 16 DSP memory, nominally used for data memory.

After the host is finished filling the DSP with boot code, the host must set the "Clear DSP Boot Mode" (Bit 3) in the DSP DMA Control Register (offset 0x1803-0x1802 from the AD1818 base

address). Setting this bit takes the DSP out of idle, and causes the DSP to start program execution from location 0x0000.

DSP INTERFACE REGISTERS

DMA Transfer Count Register

A 16-bit register contains the number of words to be transferred between PCI address space and the DSP internal memory. The word size refers to the width of transfers into the DSP internal memory. The word width may be 32 bits or 16 bits, depending on the state of the DSP Pack Mode bit in the DSP Control Register.

When the Transfer Count register reaches zero during a DMA transfer, the DMA channel is disabled. The Transfer Count register must be manually reinitialized before another DMA transfer may begin.

DMA Control Register

This register contains bits used to control and observe the state of DMA transfers to the DSP core. The control bits are read/write bits. The status bits are read-only.

Control Bits

Bit #	Description
0	Master DMA Enable. When asserted enables, PCI master DMA on the DSP DMA channel. Must be toggled off, then on to restart when DMA is disabled via the PCI address generation logic or the Transfer Count register.
1	Master DMA Write/Not Read. When asserted, specifies DMA to write to PCI address space.
2	Flush Master DMA FIFO. When asserted, discards the current contents of the DMA Master FIFO and associated logic.
3	Clear DSP Boot Mode. When asserted, forces the DSP core to begin executing instructions from the DSP internal memory. This function is valid after DSP reset.
4	Master DMA Pack Mode. Specifies the DSP internal word width for DMA transfers (1 = 32-bit words). This bit alters the semantics of the Transfer Count register.
5	D3 State Power-Down Enable. When set, allows a change to PCI power management state D3 to put the AD1818 into power-down.
6–7	Reserved.

Status Bits

Bit #	Description
8	Master DMA FIFO empty. This bit is set to one when there is no data is in the Master DMA channel FIFO or packing logic.
9	Master DMA Halt Status. This bit is set to one when the Master DMA channel is disabled by the PCI address generation logic.
15–10	Reserved

DSP Mailbox Registers

The DSP Mailbox registers are designed to allow the user to construct an efficient communications protocol between the PCI device driver and the DSP code. The mailbox functions consist of an InBox, OutBox and a control/status register.

InBox

The incoming mailbox (InBox) is 32 bits wide. It may be read or written by either the PCI device or the DSP core. The PCI device may access any or all bytes at one time. The DSP core may only access 16 bits at one time. PCI writes to the InBox may generate DSP interrupts. DSP reads of InBox may generate PCI interrupts.

OutBox

The outgoing mailbox (OutBox) is 32 bits wide. It may be read or written by either the PCI device or the DSP core. The PCI device may access any or all bytes at one time. The DSP core may only access 16 bits at one time. DSP writes to the OutBox may generate PCI interrupts. PCI reads from the OutBox may generate DSP interrupts.

Control/Status

This register consists of read/write control bits and read/write-one-clear status bits (denoted R/W and R/WC respectively). A read/write-one-clear (R/WC) bit is cleared when a one is written to it. Writing a zero has no effect.

Bit #	Type	Description
3–0	R/WC	InBox Byte Data Valid. A one in these bits means valid data has been written into the corresponding InBox bytes. The bits are cleared when they are written with ones, or when InBox is read.
7–4	R/WC	OutBox Byte Data Valid. A one in these bits means valid data has been written into the corresponding OutBox bytes. The bits are cleared when they are written with ones, or when OutBox is read.
11–8	R/O	Reserved.
12	R/WC	InBox PCI Interrupt Pending. This bit is set when the DSP reads valid data from the InBox.
13	R/WC	OutBox PCI Interrupt Pending. This bit is set when the DSP writes valid data to the OutBox.
14	R/WC	InBox DSP Interrupt Pending. This bit is set when the PCI writes valid data to the InBox.
15	R/WC	OutBox DSP Interrupt Pending. This bit is set when the PCI reads valid data from the OutBox.
16	R/W	InBox PCI Interrupt Enable. When asserted, allows the corresponding Interrupt Pending bit to be set.
17	R/W	OutBox PCI Interrupt Enable. When asserted, allows the corresponding Interrupt Pending bit to be set.
18	R/W	InBox DSP Interrupt Enable. When asserted, allows the corresponding Interrupt Pending bit to be set.
19	R/W	OutBox DSP Interrupt Enable. When asserted, allows the corresponding Interrupt Pending bit to be set.
31–20		Reserved.

PCI Memory Organization

As mentioned above, the AD1818 on-chip memory is mapped to the PCI address space. Because one of the AD1818 memory

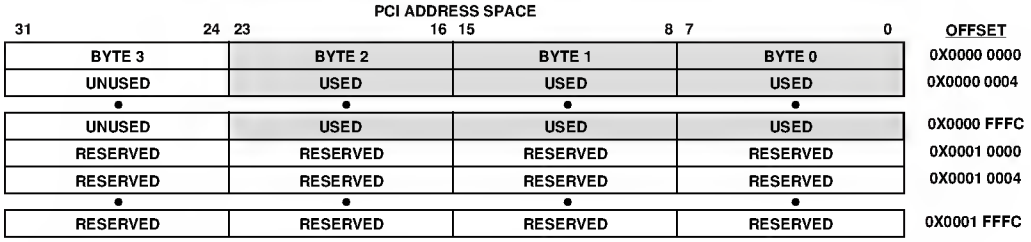


Figure 6. Footprint of AD1818 "Unpacked" 16K × 24 DSP Memory in PCI Address Space

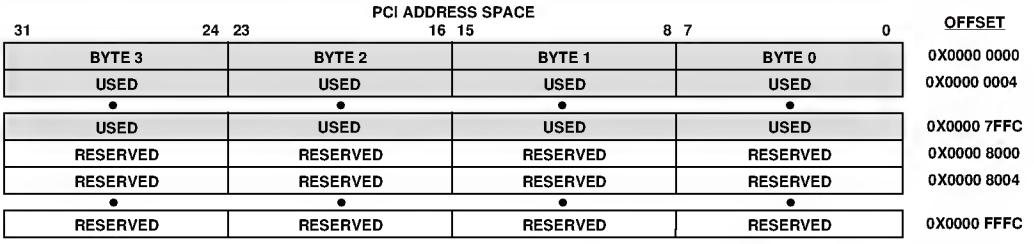


Figure 7. Footprint of AD1818 "Packed" 16K × 16 DSP Memory in PCI Address Space

blocks is 24 bits wide, and the other AD1818 memory block is 16 bits wide, there are two different "footprints" in PCI address space. The 16K by 24-bit DSP memory requests 128K bytes of "nonpacked" PCI memory. Of this, 64K bytes are reserved (for larger memory versions of the AD1818 in the future), 48K bytes are used and 16K bytes are unused. This footprint is illustrated in Figure 6.

The 16K by 16-bit DSP memory requests 64K bytes of "packed" PCI memory. Of this, 32K bytes are reserved (for larger memory versions of the AD1818 in the future) and 32K bytes are used. This footprint is illustrated in Figure 7.

Internal DSP I/O Access Addresses

Page	I/O Address	DirectSound Mixer Control Register
0	0x00	DMA Input Channel 0–3 Mixer Control
0	0x02	DMA Input Channel 4–7 Mixer Control
	. . .	
0	0x0E	DMA Input Channel 28–31 Mixer Control
0	0x1E–0x10	Reserved
0	0x22–0x20	DMA Input Channel Enable Register
0	0x3E–0x24	Reserved
0	0x40	DMA Output Channel 0 Mixer Control
0	0x42	DMA Output Channel 1 Mixer Control
	. . .	
0	0x46	DMA Output Channel 3 Mixer Control
0	0x48	DMA Output Channel Enable Register
0	0x7E–0x4A	Reserved
0	0x80	Reserved
0	0xFF–0x82	Reserved
1	0x00	DMA Input Channel 0 Attenuation
1	0x02	DMA Input Channel 1 Attenuation
	. . .	
1	0x3E	DMA Input Channel 31 Attenuation
1	0x40	Reserved
1	0x42	Reserved
1	0x44	DSP Output Channel 0 Attenuation
1	0x46	DSP Output Channel 1 Attenuation
1	0x48	Music Synthesis Attenuation
1	0x4A	AC '97 Mic Input Attenuation
1	0x4C	AC '97 Audio Input Attenuation
1	0x4E	Reserved
1	0x7E–0x50	Reserved
1	0x80	Mixer Channel 0 Input Sample Rate
1	0x82	Mixer Channel 1 Input Sample Rate
	. . .	
1	0x8E	Mixer Channel 7 Input Sample Rate
1	0x90	Reserved
1	0x92	Reserved
1	0x94	DSP Channel 0 Input Sample Rate
1	0x96	DSP Channel 1 Input Sample Rate
1	0x98	Reserved
1	0x9C–0x9A	Reserved
1	0x9E	Reserved
2	0x00	Audio Output Channel Select Register
2	0x02	Host/DSP Output Channel Select Register
2	0x1E–0x04	Reserved
2	0x20	Output Channel 0 (Variable Output) Sample Rate
9–3	0xFE–0x00	Reserved
A	0x43–0x40	DSP DMA Output Channel Base Address/ SGD Table Pointer
A	0x47–0x44	DSP DMA Output Channel Current Address/SGD CUR Pointer Address
A	0x4B–0x48	DSP DMA Output Channel Base Count/ SGD Pointer
A	0x4E–0x4C	DSP DMA Output Channel Current Count
A	0xFE–0x50	Reserved
C–B		Reserved
D	0x22–0x20	DSP DMA Output Channel Interrupt Count
D	0x26–0x24	DSP DMA Output Channel Interrupt Base Count
D	0xFE–0x24	Reserved
F	0x18–0x00	Reserved
F	0x22–0x20	DSP DMA Output Channel PCI Control Status
F	0xFF–0x24	Reserved

AC '97 Interface Registers

Page	Address	Register
10	0x7E–0x00	Register Set
10	0x80	Analog Codec Interface Control/Status
17–11		Reserved

DSP Control Registers

Page	Address	Register
18	0x00	DMA Transfer Count
18	0x02	DMA Control
18	0x06–0x04	Mailbox Control/Status
18	0x0A–0x08	Incoming Mailbox
18	0x0E–0x0C	Outgoing Mailbox

Wavetable Music Synthesis

Wavetable music synthesis algorithms are run on the internal DSP. The software wavetable engine will perform the necessary pitch shifting and envelope generation prior to mixing the channel back into the output streams.

System (PCI) memory is used for the storage of wavetable samples while the wavetable engine is in use. During application initialization, the wavetable driver will load the wavetable samples into memory for use by the AD1818. The samples need not be in contiguous memory; instead, they will be accessed by the AD1818 via scatter-gather DMA transfers. The standard DLS downloadable sounds format is supported by the AD1818 wavetable driver.

The AD1818 wavetable driver provides all of the control required for the chip to perform the necessary sample rate conversion, envelope generation and effects processing. This includes MIDI command interpretation, location of note samples in memory and passing parameters to the AD1818 for note events.

The wavetable synthesizer has been developed by Euphonics, a research and development company that specializes in audio processing and electronic music synthesis.

INTERRUPT STRUCTURE

Various flag input and output and interrupt pins within the DSP core are assigned to particular functions within the AD1818. The assignments are as follows:

PWD – Power-Down Interrupt. Connected to bit in the PCI DSP Control register.

IRQ3 – PCI Mailbox Interrupt. Writing to the incoming mailbox register or reading from the outgoing mailbox register via the PCI bus can generate this interrupt.

IRQ2 – Ring. Connected to the RING pin on the AD1818. This is an active-HIGH interrupt. Also connected without inversion to FLAGIN[3]. Used to connect to the RING signal from the DAA for modem operation. If modem is not used, can be a general purpose interrupt.

IRQ1 – Connected to external pin. General purpose interrupt.

IRQ0 – 48 kHz SYNC. Connects AD1818 DSP core to the start of frame signal. Used to time data transfers to the core for audio effects.

USER1 – FIFO2 Transmit. Connected to the transmit interrupt for the third, transmit-only FIFO.

USER0 – PCI D1 Power-Up. Connected to the PCI power management control. Used to bring the DSP out of Idle while in the D1 power state.

FLAGIN0–1 – General Purpose signals from pins.

FLAGIN3 – Ring. See above. Brought to FLAGIN for ring counting.

FLAGIN2 – Phone. From DAA.

FLAGIN4 – Reserved.

FLAGIN5 – Analog Interface Ready. Signals that the analog front-end is ready.

FLAGIN6–7 – Reserved.

FLAGOUT0–1 – General Purpose Signals to output pins.

FLAGOUT2 – Hook. Signal to DAA to connect to phone line. Can be used as a general purpose pin output signal.

FLAGOUT3 – MICENB. Signal to enable microphone. Can be used as a general purpose pin output signal.

FLAGOUT4 – PME Power-Up Request. Signal to request a PME event on the PCI bus to wake up the bus. A PME event will occur if the PME_En bit is set in the PCI configuration PMCSR register and this signal is asserted.

FLAGOUT5–7 – Reserved.

Table I. Interrupt Vector Table for the AD1818

Bit	Pri	Interrupt	Vector Address
0	1	Reset (Nonmaskable)	0x00
1	2	Power-Down (Nonmaskable)	0x04
2	3	User Interrupt 3	0x08
3	4	PCI Mailbox (IRQ3)	0x0C
4	5	Timer	0x10
5	6	User Interrupt 2	0x14
6	7	Ring (IRQ2)	0x18
7	8	IDMA	0x1C
8	9	IRQ1	0x20
9	10	FIFO0 Transmit	0x24
10	11	FIFO0 Receive	0x28
11	12	FIFO1 Transmit	0x2C
12	13	FIFO1 Receive	0x30
13	14	48 kHz SYNC (IRQ0)	0x34
14	15	FIFO2 Transmit	0x38
15	16	PCI D1 Power-Up (User 0)	0x3C

DSP to Mixer FIFOs on the AD1818

Five FIFOs provide an interface on the AD1818 between the DSP and the mixer data bus in the AD1818 core. Two of the FIFOs are inputs FIFOs, receiving data from the mixer data bus into the DSP. The other three FIFOs are transmit FIFOs, sending data from the DSP to the mixer. Each of the FIFOs are eight words deep and 16 bits wide. Interrupts to the DSP can be generated when some (programmable) number of words have been received in the input FIFOs or when some (programmable) number of words are empty in the transmit FIFOs.

The interface to the FIFOs on the DSP is simply a register interface to the IDMD bus. Tx0, Rx0, Tx1, and Rx1 are the primary FIFO registers in the universal register map of the DSP. STCTL0-2, SRCTL0-1, Tx2 and ABFCTL0-2 are the FIFO control registers and are located in the memory-mapped register space of the DSP. The FIFOs can be used to generate interrupts to the DSP based upon FIFO transactions or can initiate DMA

requests. FIFO2 uses the DMA3 controller and the USER-1 (#14) DSP interrupt.

The interface to the FIFOs on the mixer side is via the mixer address and data bus. Each of the transmit FIFOs is assigned two addresses on the mixer bus, one for left data and one for right data. Upon reset or when the transmit FIFO is disabled, zeros are driven to the mixer bus when the FIFO is addressed. When the FIFO is in mono mode, both left and right will get the same data. FIFO2 always transmits stereo data. If the transmit FIFOs run out of data then the last data shipped will continue to be sent when addressed.

The transmit FIFOs can also be used to ship data to the modem output on the analog codec (AC '97) interface. When modem mode is enabled in the transmit FIFO, it responds to the modem_out address on the mixer data bus instead of the dsp_in addresses (this applies to FIFO0 or FIFO2 only). Zeros are shipped to the mixer in modem mode. Handset audio is handled similarly. While FIFO0 or FIFO2 support modem_out, FIFO1 handles handset_out.

On the receive side, the receiver will respond to addresses that are programmed into its receive control register. Thus the receive FIFOs can collect any of the data that is sent on the mixer data bus. If stereo is enabled in the receive FIFOs, then both left and right data will be collected. In mono mode, only the left data will be collected. The data input can be from any of the rate converted output streams or from the analog codec (AC '97) interface.

Table II shows the register format for each FIFO.

Table II.

STCTL0/1 Transmit Control and Status Register

Bit	Function When Bit Set to "1"
0	Tx Enable
1	Tx Stereo Enable
2	Modem Output Enable on Mixer Channel 36 (FIFO0) Handset/Speaker Output Enable on Channel 54 (FIFO1)
3	Reserved
. . .	Bits 4 through 11 Reserved
12	Reserved
13	Transmit FIFO Full (Read Only)
14	Transmit FIFO Empty (Read Only)
15	Transmitter Empty (Read Only)

Default State After Reset: 0x00

STCTL2 Transmit-Only FIFO Control and Status Register

Bit	Function When Bit Set to "1"
0	Tx Enable (by Itself: Enables Channels 44/45)
1	Reserved
2	Modem Output Enable (On Channel 36)
3	4-Channel (with Tx Enable, Enables Channels 46/47)
4	6-Channel (with Tx Enable, Enables Channels 52/53)
5	Reserved
. . .	Bits 6 through 11 Reserved
12	Reserved
13	Transmit FIFO Full (Read Only)
14	Transmit FIFO Empty (Read Only)
15	Transmitter Empty (Read Only)

Default State After Reset: 0x00

SRCTL0/1 Transmit-Only FIFO Control and Status Register

Bit	Function When Bit Set to "1"
0	Rx Enable
1	Rx Stereo Enable
2	Rx Select Address (LSB)
3	Rx Select Address
4	Rx Select Address
5	Rx Select Address
6	Rx Select Address (MSB)
7	Reserved
. . .	Bits 8 through 11 Reserved
12	Reserved
13	Receive FIFO Full (Read Only)
14	Receive FIFO Empty (Read Only)
15	Receiver Full (Read Only)

Default State After Reset: 0x00

ABFCTL0/1 DMA and FIFO Control Register

Bit	Function When Bit Set to "1"
0	Tx FIFO Enable
1	Rx FIFO Enable
2	Reserved
3	Reserved
4	Tx FIFO Interrupt Position (LSB)
5	Tx FIFO Interrupt Position
6	Tx FIFO Interrupt Position (MSB)
7	Reserved
8	Rx FIFO Interrupt Position (LSB)
9	Rx FIFO Interrupt Position
10	Rx FIFO Interrupt Position (MSB)
11	Reserved
12	Tx DMA Enable
13	Reserved
14	Rx DMA Enable
15	Reserved

Default State After Reset: 0x00

ABFCTL2 DMA and FIFO Control Register

Bit	Function When Bit Set to "1"
0	Tx FIFO Enable
1	Reserved
2	Reserved
3	Reserved
4	Tx FIFO Interrupt Position (LSB)
5	Tx FIFO Interrupt Position
6	Tx FIFO Interrupt Position (MSB)
7	Reserved
. . .	Bits 8 through 10 Reserved
11	Reserved
12	Tx DMA Enable
13	Reserved
14	Reserved
15	Reserved

The FIFOs also use the DSP core registers Tx buffer and Rx buffer. FIFO2's Tx register is a sysctll register, reg (0xlA) = reg(tx2). There is a total of 4 "memory-mapped" registers per DSP serial port (SPORT).

DirectSound Output Channel to Select Channel Matching

Select	Data Stream	Transaction Source	Data Source
0	DS[0]	Rate Converter/48 kHz	Rate Converter
1	DS[1]	Rate Converter/48 kHz	Rate Converter
2	DS[2]	Rate Converter/48 kHz	Rate Converter
3	DS[3]	Rate Converter/48 kHz	Rate Converter
4	DS[4]	Rate Converter/48 kHz	Rate Converter
5	DS[5]	Rate Converter/48 kHz	Rate Converter
6	DS[6]	Rate Converter/48 kHz	Rate Converter
7	DS[7]	Rate Converter/48 kHz	Rate Converter
8	Reserved		
9	Reserved		
A	dsp_out[0]	Rate Converter/48 kHz	Rate Converter
B	dsp_out[1]	Rate Converter/48 kHz	Rate Converter
C	Music Synth	Rate Converter/48 kHz	Rate Converter
D	var_out	Rate Converter/Variable	Rate Converter
E	audio out	Rate Converter/48 kHz	Rate Converter
F	hdsp_out	Rate Converter/48 kHz	Rate Converter
10	audio_in	AC '97/48 kHz	AC '97
11	modem_in	AC '97/Variable	AC '97
12	modem_out	AC '97/Variable	AC '97
13	mic_in	AC '97/Variable	AC '97
14	dsp_from[0]	Rate Converter/Variable	DSP
15	dsp_from[1]	Rate Converter/Variable	DSP
16	dsp_2_acif[0]	AC '97/Variable	DSP
17	dsp_2_acif[1]	AC '97/Variable	DSP
18	reserved		
19	reserved		
1A	dsp_2_acif[2]	AC '97/Variable	DSP
1B	handset	AC '97/ Variable	DSP
1C	music synth_in	Rate Converter/22.05 kHz	Music Synthesizer
1D	Reserved		
1E	Reserved		
1F	Reserved		

PCI INTERFACE

In order to support the high data throughput required for concurrent audio and telephony algorithms, the AD1818 includes a 33 MHz, 32-bit bus master 5 V PCI interface. The interface is compliant with revision 2.1 of the PCI specification, and the AD1818 is memory-mapped to the PCI bus.

THE AD1818 LOGICAL DEVICE

The DirectSound Mixer block provides the PCI interface necessary for the 64-stream Mixer block. This interface supports the use of system memory for storage of wavetable samples and envelopes. On-chip FIFOs provide the buffering needed to support high throughput on the PCI bus and samples as needed for the wavetable synthesizer. Scatter-gather capability is provided for each DMA channel. A MIDI MPU-401 interface to the MIDI IN and MIDI OUT pins is also provided by this logical device.

The AC '97 interface is the primary interface to the main analog codec front-end. A FIFO buffers data to and from the serial codec interface.

The PCI interface to the on-chip DSP provides both master and slave burst capability between system memory and the on-chip DSP memory. Separate target addressing is provided for the 24-bit DSP program memory space and the 16-bit DSP data memory space. Bus master DMA can be controlled by either the DSP through an internal interface or the host via the PCI interface. Separate data FIFOs exist for target and master transfers.

SCATTER-GATHER DMA ON THE AD1818

When Direct Memory Access (DMA) is active, it will "steal" one cycle from the DSP core for each transfer that takes place. During the DMA transfer, no other DSP core activity occurs. When transferring audio samples to the wavetable engine or the codec engine, the DMA transfer can be programmed to perform scatter-gather DMA. This mode allows the audio samples to be split up in memory, and yet able to be transferred to and from the AD1818 without processor intervention. In Scatter-Gather mode, the DMA controller can read the memory address and word count from an array of buffer descriptors called the Scatter-Gather Descriptor (SGD) table. This allows the DMA engine to sustain DMA transfers until all buffers in the Scatter-Gather Descriptor table are transferred.

To initiate a Scatter-Gather transfer between memory and the AD1818, the following steps are involved:

1. Software driver prepares a SGD table in system memory. Each Scatter-Gather Descriptor (SGD) is eight bytes long and consists of an address pointer to the starting address and the transfer count of the memory buffer to be transferred. In any given SGD table, two consecutive SGDs are offset by eight bytes and are aligned on a 4-byte boundary. Each SGD contains:
   a. Memory Address (Buffer Start) – 4 Bytes
   b. Byte Count (Buffer Size) – 3 Bytes
   c. End of Linked List (EOL) – 1 Bit (MSB)
   d. Flag – 1 Bit
2. Initialize DMA control registers with transfer specific information such as bit width, compression mode, etc.
3. Software driver initializes the hardware pointer to the SGD table.
4. Engage Scatter-Gather DMA by writing the Start value to the Scatter-Gather Command register.
5. The AD1818 will then pull in samples as pointed to by the Scatter-Gather descriptors as needed by the audio synthesis engine. When the End of Linked List (EOL) is reached, a status bit will be set and the DMA will end if the sample is not to be looped. If looping is to occur, DMA transfers will continue from the beginning of the sample until a Stop command is received in the Scatter-Gather command register.
6. Bits in the Scatter-Gather command register control whether or not an interrupt occurs when the End of Linked List is reached or when the flag bit is set.

PCI Configuration Space Organization for the AD1818

The AD1818 contains a single Configuration Space with six separate address spaces pointed to by address registers in that configuration space. The function is logical device 0. All of the AD1818 address spaces (including the Configuration Space) are memory-mapped to the PCI bus.

CONFIGURATION SPACE REGISTER DEFINITION

Configuration Space Register Map

Address	Register	Comments
0x01–0x00	Vendor ID	Hardwired – 0x11D4
0x03–0x02	Device ID	Hardwired – 0x1818
0x05–0x04	Command Register	Reset to 0, See Note (a)
0x07–0x06	Status Register	See Note (b)
0x08	Revision ID	Hardwired – 0x00
0x0B-0x09	Class Code	Hardwired – 0x040100
0x0C	Cache Line Size	Unimplemented
0x0D	Latency Timer	R/W, Reset to 0
0x0E	Header Type	Hardwired to 0
0x0F	BIST	Unimplemented
0x13–0x10	Base Address 0	8K Bytes Prefetchable DirectSound, Codec, DSP Registers
0x17–0x14	Base Address 1	16 Bytes Nonprefetchable Music Synthesis Registers
0x1B–0x18	Base Address 2	16 Bytes Nonprefetchable MIDI MPU-401 Interface
0x1F–0x1C	Base Address 3	16 Bytes Nonprefetchable Legacy Control Interface
0x23–0x20	Base Address 4	128K Bytes Prefetchable 24-Bit DSP Memory
0x27–0x24	Base Address 5	64K Bytes Prefetchable. 16-bit DSP Memory
0x2B–0x28	Cardbus CIS Pointer	Unimplemented
0x2D–0x2C	Subsystem Vendor ID	Reset to 0x11D4
0x2F–0x2E	Subsystem ID	Reset to 0x1818
0x33–0x30	Expansion ROM Base Address	Unimplemented
0x34	Capability Pointer	Hardwired – 0xDC
0x3B–0x35	Reserved in PCI Spec	Unimplemented
0x3C	Interrupt Line	R/W, Reset to 0
0x3D	Interrupt Pin	Hardwired – 0x01 (Uses INTA#)
0x3E	Min_Gnt Register	Hardwired – 0x01
0x3F	Max_Lat Register	Hardwired – 0x0A
0xDB–0x40		Unimplemented
0xDC	Capability ID	Hardwired – 0x01
0xDD	Next_Cap_Ptr	Hardwired – 0x00
0xDF–0xDE	Power Management Cap	Hardwired – 0x1321
0xE1–0xE0	Power Mgmt. Ctrl/Stat	Reset to 0
0xE2	Power Mgmt. Bridge	Hardwired to 0
0xE3	Power Mgmt. Data	Hardwired to 0
0xFF–0xE4	Configuration Space	

Configuration Space Notes

(a) Command Register Bits:

0 – I/O Space Enable	Hardwired to 0, All Accesses Are via Memory Space
1 – Memory Space Enable	Reset to 0
2 – Bus Master Enable	Reset to 0
3 – Special Cycle Enable	Hardwired to 0
4 – MWI Enable	Unimplemented, Hardwired to 0
5 – VGA Palette Snoop	Unimplemented, Hardwired to 0
6 – Parity Error Response	Reset to 0
7 – Address/Data Stepping	Hardwired to 0
8 – SERR# Enable	Reset to 0
9 – Fast Back-to-Back	Reset to 0
15–10	Hardwired to 0

(b) Status Register Bits:

3–0	Hardwired to 0
4 – Capabilities List	Hardwired to 1
5 – 66 MHz Capable	Hardwired to 0
6 – UDF Supported	Hardwired to 0
7 – Fast B2B Capable	Hardwired to 1
8 – Data Parity Error Detect	Implemented, Reset to 0
10–9 – Devsel Timing	Hardwired to 01 – Medium Speed
11 – Signaled Target Abort	Implemented, Reset to 0
12 – Received Target Abort	Implemented, Reset to 0
13 – Received Master Abort	Implemented, Reset to 0
14 – Signaled System Error	Implemented, Reset to 0
15 – Detected Parity Error	Implemented, Reset to 0

Unimplemented configuration space reads back 0s onto the PCI bus if accessed, by default. PCI writes to these locations have no effect.

PCI MEMORY SPACE REGISTER DEFINITION

Top-Level Base Address Offsets:

DirectSound – Offset from Base Address 0:

Address	Register
0x07FF–0x0000	Mixer Control Registers
0x0FFF–0x0800	DMA Registers
0x17FF–0x1000	AC '97 Interface Registers
0x1FFF–0x1800	DSP Control Registers

Music Synthesis – Offset from Base Address 1:

Address	Register
0x00	OPL3 Music0: Address (w), Status (r)
0x01	OPL3 Music0: Data
0x02	OPL3 Music1: Address (w)
0x03	OPL3 Music1: Data
0x0F–0x04	Reserved

MIDI MPU-401 – Offset from Base Address 2:

Address	Register
0x00	MIDI Data (r/w)
0x01	MIDI UART Status (r), Command (w)
0x0F–0x02	Reserved

Legacy Control – Offset from Base Address 3:

Address	Register
0x00	Legacy Audio Control/Status.
0x0F–0x01	Reserved

DSP Port – Offset from Base Address 4:

Address	Register
0x1FFFF–0x00	24-bit DSP memory

DSP Port – Offset from Base Address 5:

Address	Register
0xFFFF–0x00	16-bit DSP memory

Base Address 0 Register Detail:

DirectSound Mixer Control Registers

Address	Register
0x001–0x000	DMA Input Channel 0–3 Mixer Control
0x003–0x002	DMA Input Channel 4–7 Mixer Control
. . .	
0x00F	DMA Input Channel 28–31 Mixer Control
0x01F–0x010	Reserved
0x023–0x020	DMA Input Channel Enable Register
0x03F–0x024	Reserved
0x041–0x040	DMA Output Channel 0 Mixer Control
. . .	
0x047–0x046	DMA Output Channel 3 Mixer Control
0x049–0x048	DMA Output Channel Enable Register
0x0FF–0x04A	Reserved
0x101–0x100	DMA Input Channel 0 Attenuation
0x103–0x102	DMA Input Channel 1 Attenuation
. . .	
0x13F–0x13E	DMA Input Channel 31 Attenuation
0x143–0x140	Reserved
0x145–0x144	DSP Output Channel 0 Attenuation
0x147–0x146	DSP Output Channel 1 Attenuation
0x149–0x148	OPL3 Music Synthesis Attenuation
0x14B–0x14A	AC '97 Mic Input Attenuation
0x14D–0x14C	AC '97 Audio Input Attenuation
0x17F–0x14E	Reserved
0x181–0x180	Mixer Channel 0 Input Sample Rate
0x183–0x182	Mixer Channel 1 Input Sample Rate
. . .	
0x18F–0x18E	Mixer Channel 7 Input Sample Rate
0x193–0x190	Reserved
0x195–0x194	DSP Channel 0 Input Sample Rate
0x197–0x196	DSP Channel 1 Input Sample Rate
0x19F–0x198	Reserved
0x201–0x200	Audio Output Channel Select Register
0x203–0x202	Host/DSP Output Channel Select Register
0x21F–0x204	Reserved
0x221–0x220	Output Channel 0 (Variable Output) Sample Rate
0x7FF–0x222	Reserved

DirectSound DMA Registers

Address	Register
0x803–0x800	DMA Input Channel 0 Base Address / SGD Table Pointer
0x807–0x804	DMA Input Channel 0 Current Address / SGD CUR Pointer Address
0x80B–0x808	DMA Input Channel 0 Base Count / SGD Pointer
0x80F–0x80C	DMA Input Channel 0 Current Count
0x813–0x810	DMA Input Channel 1 Base Address / SGD Table Pointer
0x817–0x814	DMA Input Channel 1 Current Address / SGD CUR Pointer Address
0x81B–0x818	DMA Input Channel 1 Base Count / SGD Pointer
0x81F–0x81C	DMA Input Channel 1 Current Count
. . .	
0x9F3–0x9F0	DMA Input Channel 31 Base Address / SGD Table Pointer
0x9F7–0x9F4	DMA Input Channel 31 Current Address / SGD CUR Pointer Address
0x9FB–0x9F8	DMA Input Channel 31 Base Count / SGD Pointer
0x9FF–0x9FC	DMA Input Channel 31 Current Count
0xA03–0xA00	DMA Output Channel 0 Base Address / SGD Table Pointer
0xA07–0xA04	DMA Output Channel 0 Current Address / SGD CUR Pointer Address
0xA0B–0xA08	DMA Output Channel 0 Base Count / SGD Pointer
0xA0F–0xA0C	DMA Output Channel 0 Current Count
. . .	
0xA33–0xA30	DMA Output Channel 3 Base Address / SGD Table Pointer
0xA37–0xA34	DMA Output Channel 3 Current Address / SGD CUR Pointer Address
0xA3B–0xA38	DMA Output Channel 3 Base Count / SGD Pointer
0xA3F–0xA3C	DMA Output Channel 3 Current Count
0xA43–0xA40	DSP DMA Output Channel Base Address / SGD Table Pointer
0xA47–0xA44	DSP DMA Output Channel Current Address / SGD CUR Pointer Address
0xA4B–0xA48	DSP DMA Output Channel Base Count / SGD Pointer
0xA4F–0xA4C	DSP DMA Output Channel Current Count
0xBFF–0xA50	Reserved
0xC02–0xC00	DMA Input Channel 0 Interrupt Count
0xC03	Reserved
0xC06–0xC04	DMA Input Channel 0 Interrupt Base Count
0xC07	Reserved
0xC0A–0xC08	DMA Input Channel 1 Interrupt Count
0xC0B	Reserved
0xC0E–0xC0C	DMA Input Channel 1 Interrupt Base Count
0xC0F	Reserved
. . .	
0xCFA–0xCF8	DMA Input Channel 31 Interrupt Count
0xCFB	Reserved
0xCFE–0xCFC	DMA Input Channel 31 Interrupt Base Count
0xCFF	Reserved
0xD02–0xD00	DMA Output Channel 0 Interrupt Count
0xD03	Reserved
0xD06–0xD04	DMA Output Channel 0 Interrupt Base Count
0xD07	Reserved
. . .	
0xD1A–0xD18	DMA Output Channel 3 Interrupt Count
0xD1B	Reserved
0xD1E–0xD1C	DMA Output Channel 3 Interrupt Base Count
0xD1F	Reserved
0xD22–0xD20	DSP DMA Output Channel Interrupt Count
0xD23	Reserved
0xD26–0xD24	DSP DMA Output Channel Interrupt Base Count
0xD27	Reserved
0xDFF–0xD28	Reserved
0xE03–0xE00	DMA Input Channel 0 PCI Control/Status
0xE07–0xE04	Reserved
0xE0B–0xE08	DMA Input Channel 1 PCI Control/Status
0xE0F–0xE0C	Reserved
. . .	
0xEFB–0xEF8	DMA Input Channel 31 PCI Control/Status
0xEFF–0xEFC	Reserved
0xF03–0xF00	DMA Output Channel 0 PCI Control/Status

0xF07–0xF04	Reserved
. . .	
0xF1B–0xF18	DMA Output Channel 3 PCI Control/Status
0xF1F–0xF1C	Reserved
0xF23–0xF20	DSP DMA Output Channel PCI Control/Status
0xF27–0xF24	Reserved
0xF7F–0xF28	Reserved
0xF83–0xF80	DMA Interrupt Register 1
0xF87–0xF84	DMA Interrupt Register 2
0xF8B–0xF88	DMA Channel Stop Status Register 1
0xF8F–0xF0C	DMA Channel Stop Status Register 2
0xFFF–0xF90	Reserved

AC '97 Codec Interface Registers

Address	Register
0x107F–0x1000	AC '97 Register Set
0x1081–0x1080	Analog Codec Interface Control/Status
0x17FF–0x1082	Reserved

DSP Control Registers

Address	Register
0x1801–0x1800	DMA Transfer Count
0x1803–0x1802	DMA Control
0x1807–0x1804	Mailbox Control/Status
0x180B–0x1808	Incoming Mailbox
0x180F–0x180C	Outgoing Mailbox

Control Register Definitions:

***DMA Input Channel Mixer Control Registers* (8):**

Bit #	Description
3–0	Even Channel Data Format
7–4	Odd Channel Data Format
31–8	Reserved

Data Format Definition:

Bit #	Description
0	S/M – Stereo/Mono Select (Mono = 0, Stereo = 1)
1	C/L – Companded/Linear Select (Linear = 0, Companded = 1)
2	FMT – Format Select (μ-Law/8-Bit Data = 0, A-Law/16-Bit Data = 1)
3	Reserved

DMA Input Channel Enable Register (1):

Bit #	Description
0	Input Channel 0 Enable
1	Input Channel 1 Enable
. . .	
31	Input Channel 31 Enable

Output Channel Mixer Control Registers (4):

Bit #	Description
3–0	Channel Data Format
7–4	Reserved
12–8	Mixer Output Select
16–13	Reserved

Data Format definition is defined above.

Mixer Output Select is a 5-bit value, which selects one channel as follows:

DirectSound Channel 0	0
DirectSound Channel 1	1
. . .	
DirectSound Channel 7	7
Reserved	8
Reserved	9
DSP FIFO 0	10
DSP FIFO 1	11
OPL3 Music Synthesis	12
Output Channel 0	13
AD1818 Audio Output (Primary)	14
AD1818 Host/DSP Output (Secondary)	15
AC '97 Audio In	16
AC '97 Modem In	17
AC '97 Modem Out	18
AC '97 Mic In	19
Reserved	20–31

DMA Output Channel Enable Register (1):

Bit #	Description
0	Output Channel 0 Enable
1	Output Channel 1 Enable
. . .	
3	Output Channel 3 Enable
15–4	Reserved

Channel Attenuation Registers (37):

Bit #	Description
5–0	Left Attenuation
6	Reserved
7	Left Mute
13–8	Right Attenuation
14	Reserved
15	Right Mute

Each channel attenuation bit is weighted 1.5 dB.

Mixer/DSP Input/Output Sample Rates (10):

Sample Rate (16 bits)

Output Channel Select Register (2):

Bit #	Description
7–0	Mixer Output Selects
8	Reserved
9	Reserved
10	DSP FIFO 0 Select
11	DSP FIFO 1 Select
12	OPL3 Music Synthesis Select
13	AC '97 Mic Input Select
14	AC '97 Audio Input Select
15	Reserved

Output Channel 0 Sample Rate (1):

Sample Rate (16 Bits)

DMA Channel PCI Control/Status Registers:

Bit #	Description
0	SGD Enable
1	Loop Enable
3–2	Interrupt Mode: 00 Interrupt Disabled 01 Interrupt on Count 10 Interrupt on SGD Flag 11 Interrupt on EOL
5–4	Current SGD Valid 00 Full SGD Descriptor Needed (Software Must Initialize This Value) 01 Partial SGD Descriptor Fetched 10 SGD Valid 11 Reserved (Invalid Status)
6	Flag Bit Set in Current SGD
7	EOL Bit Set in Current SGD

DMA Interrupt Register 1

Bit #	Description
0	DMA Input Channel 0 Interrupt
1	DMA Input Channel 1 Interrupt
. . .	
31	DMA Input Channel 31 Interrupt

DMA Interrupt Register 2

Bit #	Description
0	DMA Output Channel 0 Interrupt
1	DMA Output Channel 1 Interrupt
2	DMA Output Channel 2 Interrupt
3	DMA Output Channel 3 Interrupt
4	DSP DMA Channel Interrupt
13–5	Reserved
14	PCI Target Abort Interrupt
15	Master Abort Interrupt
16	PCI Target Abort Interrupt Enable
17	Master Abort Interrupt Enable
31–18	Reserved

DSP DMA Control Register Definition

Bit #	Description
0	DMA Enable
1	DMA Write/$\overline{\text{Read}}$
2	Flush Master FIFO
3	Clear DSP Boot Mode
4	DMA Packing Enable
5	D3 Power-Down Enable
7–6	Reserved
8	DMA Channel Halt Status (1 = Halt)
9	DMA FIFO Empty Status (1 = Empty)
15–10	Reserved

Mailbox Control/Status Register Definition

Bit #	Description
3–0	Incoming Mailbox Full (MSB:LSB) (R/WC)
7–4	Outgoing Mailbox Full (MSB:LSB) (R/WC)
11–8	Reserved
12	Incoming Mailbox PCI Interrupt Pending (R/WC)
13	Outgoing Mailbox PCI Interrupt Pending (R/WC)
14	Incoming Mailbox DSP Interrupt Pending (R/WC)
15	Outgoing Mailbox DSP Interrupt Pending (R/WC)
16	Incoming Mailbox PCI Interrupt Enable (R/W)
17	Outgoing Mailbox PCI Interrupt Enable (R/W)
18	Incoming Mailbox DSP Interrupt Enable (R/W)
19	Outgoing Mailbox DSP Interrupt Enable (R/W)
31–20	Reserved

Analog Codec Interface Control/Status Register:

Bit #	Description
0	Analog Codec Interface Enable
1	Analog Codec Reset Disable
2	Audio Stream Output Enable
3	AD1819/ AC '97 Mode
5–4	AD1819 DSP Audio Output Control
6	AD1819 Modem I/O Enable
7	AD1819 Handset I/O Enable
8	Force SDATA_OUT High
9	Force SYNC High
14–10	Reserved
15	Analog Codec Ready Status (RO)

Legacy Audio Control/Status Register:

Bit #	Description
0	MIDI Interrupt Enable
1	Subsystem ID Write Enable
3–2	Reserved
5–4	Music Synthesizer Test Mode
6	Reserved
7	MIDI Interrupt Pending (RO)

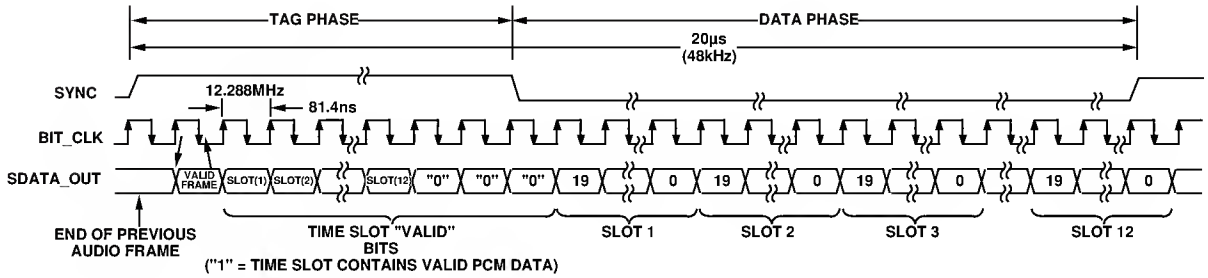


Figure 8. Time-Slot-Based AC Link Protocol

ANALOG/DIGITAL INTERFACE

Analog/Digital AC '97 Protocol

For complete information on AC '97, please refer to the Analog Devices' AD1819 data sheet.

AC '97 incorporates a 5-pin digital serial interface that links it to the AD1818. AC Link is a bidirectional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC Link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. The AD1818 provides and accepts data with 16-bit resolution.

Synchronization of all AC Link data transactions is signaled by the AD1818. The AC '97 codec drives the serial bit clock onto the AC Link, which the AD1818 then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC Link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC Link data, the AC '97 codec for outgoing data and the AD1818 for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC Link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of Slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream and contains valid data. If a slot is "tagged," it is the responsibility of the source of the data for that slot (the AC '97 codec for the input stream, digital controller for the output stream) to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase." The remainder of the audio frame where SYNC is low is defined as the "Data Phase."

Additionally, for power savings, all clock, sync and data signals can be halted. This requires that the AC '97 codec be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

AC Link Audio Output Stream (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the AC '97's DAC inputs and control registers. As briefly mentioned earlier, each audio frame supports up to twelve 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits used for AC Link protocol infrastructure.

Within Slot 0, the first bit is a global bit (SDATA_OUT Slot 0 Bit 15) that flags the validity of the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12-bit position sampled by the AC '97 indicates which of the corresponding 12 time slots contain valid data. In this way, data streams of differing sample rates can be transmitted across Link at its fixed 48 kHz sync rate. Figure 8 illustrates the time-slot- based AC Link protocol.

A new audio output frame begins with a low to high transition of SYNC (see Figure 9). SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC '97 samples the assertion of SYNC. This falling edge marks the time when both sides of the AC Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 controller transitions SDATA_OUT into the first bit position of Slot 0 (valid frame bit). Each new bit position is presented to the AC Link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATA_OUT's composite stream is MSB justified (MSB first) with all nonvalid slots' bit positions stuffed with 0s by the AD1818.

For all valid slots, the AD1818 provides 16 valid data bits and stuffs 0s in the nonvalid trailing bit positions.

Slot 1: Command Address Port

The command port is used to control fractures, and monitor status (see Audio Input Frame Slots 1 and 2) for AC '97 functions including, but not limited to, mixer settings and power management.

The control interface architecture supports up to 64 16-bit read/write registers. Audio Output Frame Slot 1 stream communicates control register address and write/read command information to the AC '97.

Command Address Port Bit Assignments:

Bit (19)	write/read command	(1 = read, 0 = write)
Bit (18:12)	Control Register Index	(64 16-bit locations, addressed on even byte boundaries)
Bit (11:0)	Reserved	(Stuffed with 1s)

The first bit (MSB) sampled by the AC '97 indicates whether the current control transaction is a read or write operation. The following seven-bit positions communicate the targeted control register address. The trailing 12-bit positions within the slot are reserved and are stuffed with 0s by the AD1818.

Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1 Bit 19).

Command Data Port Bit Assignments:

Bit (19:4)	Control Register Write Data	(Stuffed with 0s if current operation is a read)
Bit (3:0)	Reserved	(Stuffed with 0s)

Slots 3–12: Data Input Channels

Slots 3 through 12 are data input channels assigned to audio or modem streams as defined by the Analog Codec Interface Control/ Status Register in the AD1818. Each slot is defined as follows:

Data Output Bit Assignments:

Bit (19:4)	Output Data	(Stuffed with 0s if current slot is invalid)
Bit (3:0)	Reserved	(Stuffed with 0s)

AC Link Audio Input Stream (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AD1818. As in the case for the audio output stream, each AC Link audio input frame consists of 12 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits used for AC Link protocol infrastructure.

Within Slot 0, there is a global bit (SDATA_OUT Slot 0 Bit 15), which flags whether the AC '97 is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that the AC '97 is not ready for normal operation. This condition is normal following the deassertion of power on reset, for example, while the AC '97's voltage references settle. When the AC Link "Codec Ready" indicator bit is a 1, it indicates an AC '97 control. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12-bit position sampled by the AC '97 indicates which of the corresponding 12 time slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC Link at its fixed 48 kHz SYNC rate. Figure 8 illustrates the time-slot-based AC Link protocol.

If the AC '97 is sampled "Codec Ready," the next 12-bit positions sampled by the AD1818 indicate which of the corresponding 12 audio input slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC Link at its fixed 48 kHz SYNC rate.

A new audio input frame begins with a low-to-high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC '97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC Link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC '97 transitions SDATA_IN into the first bit position of Slot 0 ("Codec Ready" bit). Each new bit position is presented to AC Link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

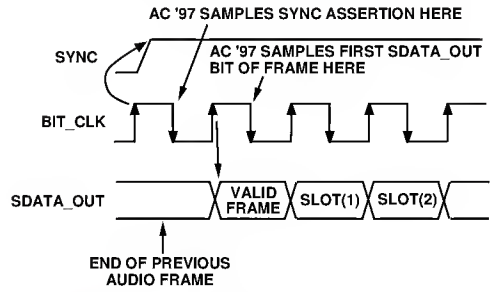


Figure 9. Start of an Audio Output Frame

SDATA_IN's composite stream is MSB justified (MSB first) with all nonvalid bit positions stuffed with 0s by the AC '97. SDATA_IN data is sampled on the falling edges of BIT_CLK .

Slot 1: Status Address Port

The status port is used to monitor status for AC '97 functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in Slot 2. (Assuming that Slots 1 and 2 had been tagged valid by the AC '97 during slot 0.)

Status Address Port Bit Assignments:

Bit (19)	Reserved	(Stuffed with 0s)
Bit (18:12)	Control Register Index	(Echo of register index for which data is being returned)
Bit (11:0)	Reserved	(Stuffed with 0s)

The first bit (MSB) generated by the AC '97 is always stuffed with a 0. The following seven bit positions communicate the associated control register address and the trailing 12 bit positions are stuffed with 0s by the AC '97.

Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Status Data Port Bit Assignments:

Bit (19:4)	Control Register Read Data	(Stuffed with 0s if tagged invalid by the AC '97)
Bit (3:0)	Reserved	(Stuffed with 0s)

Slots 3–12: Data Input Channels

Slots 3 through 12 are data input channels assigned to audio or modem streams as defined by the Analog Codec Interface Control/Status Register in the AD1818. Each slot is defined as follows:

Data Input Bit Assignments:

Bit (19:4)	Input Data	(Stuffed with 0s if tagged invalid by the AC '97)
Bit (3:0)	Reserved	(Stuffed with 0s)

Analog Codec Interface Control

There are several configurations in which the analog Codec interface can work. These configurations are controlled by the bits in the Analog Codec Interface Control/Status Register. Bits in this register enable and reset the interface and control data transfers to an AD1819 or other AC '97 compatible codec. The register can be accessed from the host through the PCI interface and from the DSP. This register is shown below:

Analog Codec Interface Control/Status Register:

Bit 0	Analog Codec Interface Enable
Bit 1	Analog Codec Reset Disable
Bit 2	Audio Stream Output Enable
Bit 3	AD1819/AC '97-Mode
Bit 5:4	AD1819 DSP Audio Output Control
Bit 6	AD1819 Modem I/O Enable
Bit 7	AD1819 Handset I/O Enable
Bit 8	Force SDATA_OUT High
Bit 9	Force SYNC High
Bit 15	Analog Codec Ready Status (RO)

The Codec Interface Enable (Bit 0) is the primary enable for the AD1818 interface to the AC Link. Setting this bit will turn on interface to use the external BIT_CLK signal coming in on the link. Therefore, Bit 0 should be enabled after reset on the AC Link has been disabled by setting Bit 1 in this register. Turning on this bit will pull the RESET# pin high (inactive) on the AC Link, thus enabling the BIT_CLK outputs on the AC '97 Codec.

Once the interface is out of reset and enabled, the codec should be ready before any data or control words are sent to the codec. The AD1818 monitors the Codec Ready status of the interface and reflects it in Bit 15 of this register. This status signal is also available to the DSP as flag input Bit 5. Codec ready going high (active) signals that register transactions between the AD1818 and the codec can occur.

Registers on the codec can be written and read by the host through the PCI interface and by the DSP. The codec registers are seen by the host at memory locations 0x1000 to 0x107F offset from Base Address Register 0. These registers are accessible from the DSP on I/O page 0x10, locations 0x00 to 0x7F.

Once the codec has been enabled and the mode of operation set, data can begin to be sent to the interface. For standard AC '97 operation, the Audio Stream Output Enable should be set and the AD1819/AC '97-Mode bit left low. With the Audio Stream Output Enable set, data from the Primary Summer mixer output will be sent to the codec at a 48 kHz sample rate.

For extended functionality when using multiple AD1819 codecs, Bits 3 through 7 in the Analog Codec Interface Control Register are used to control the system setup. With multiple AD1819 codecs, AD1818 can be programmed to send six channels of audio for Surround Sound (3 AD1819s), or two audio channels plus modem data and handset channels (two AD1819s), or other combinations.

Overall AD1819 operating modes are enabled by setting the AD1819 mode (Bit 3) high. This enables all of the rest of the control bits associated with the AD1819.

In AD1819 mode, there are two potential sources of audio data: the Primary Summer mixer output or the DSP via FIFO #2. Mixer output is enabled by setting the Audio Stream Output Enable bit. If the DSP is to generate the audio data, then the Audio Stream Output Enable bit should be low and the AD1819 DSP Audio Output Control (Bits 5-4) used to control the number of audio channels to be shipped to the AD1819s as shown below:

Bits 5:4 # of 1819 DSP Audio Channels

00 No Audio Channels (Use Mixer If Enabled)
01 2 Audio Channels from DSP to AD1819
10 4 Audio Channels from DSP to AD1819
11 6 Audio Channels from DSP to AD1819

Bits 6 and 7 in the Analog Codec Interface Control Register control the AD1819 Modem and Handset I/O Enables, respectively. Modem and handset data generally is shipped to and from the DSP to the codec interface. Control bits in the DSP to Mixer FIFOs control which FIFOs send and receive the modem and handset data.

When multiple AD1819s are used in a system with the AD1818, there are requirements on the functionality performed by the master AD1819. (See the AD1819 Data Sheet for more information on codec master and slave organization.) When mixer audio output is enabled, audio data is shipped on the first two data channels in each frame, thus the master codec must be used as the audio codec. Any modem data would be transferred on later channels, and thus the modem must be the slave codec. When the DSP is used to supply audio data, however, the modem data is shipped in the first two channels, therefore going to the master codec. The DSP can ship two or four channels of audio when modem is enabled. These channels will go in successive slots to slave codecs 1 or 2.

Bits 8 and 9 in the Analog Codec Interface Control Register are used for test modes to control the SYNC and SDATA_OUT pins. For normal operation they must be cleared.

ELECTRICAL SPECIFICATIONS

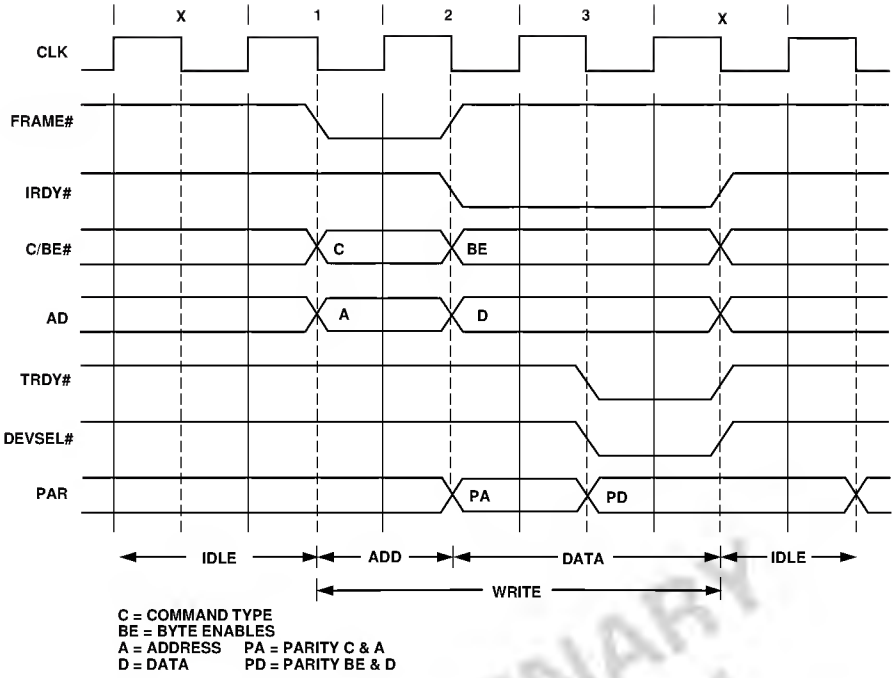


Figure 10. Slave Single Write Access Cycle (Medium Speed Decode)

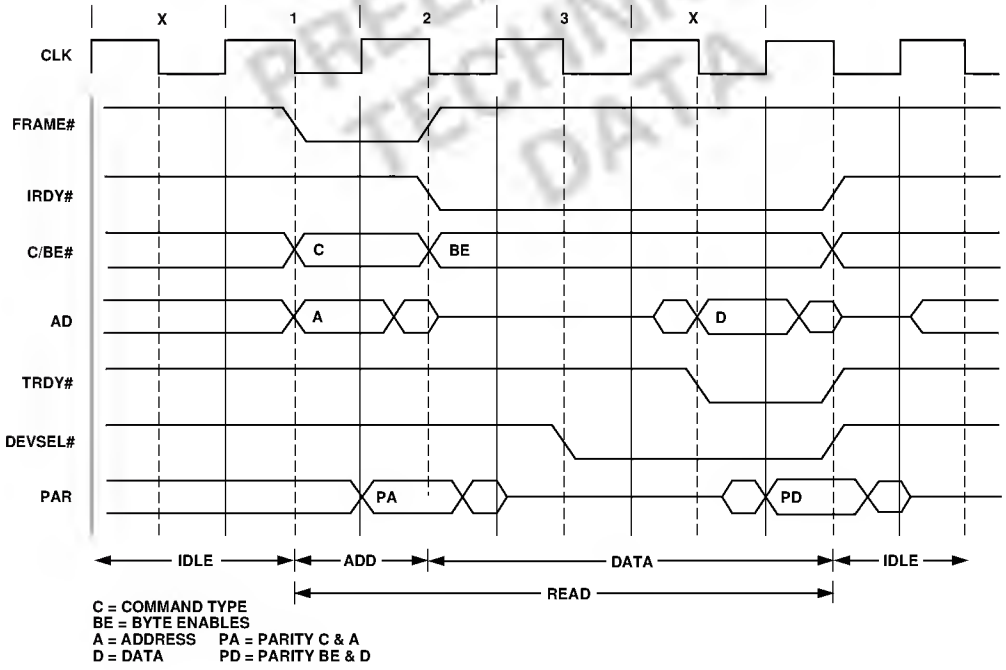


Figure 11. Slave Single Read Access Cycle (Medium Speed Decode)

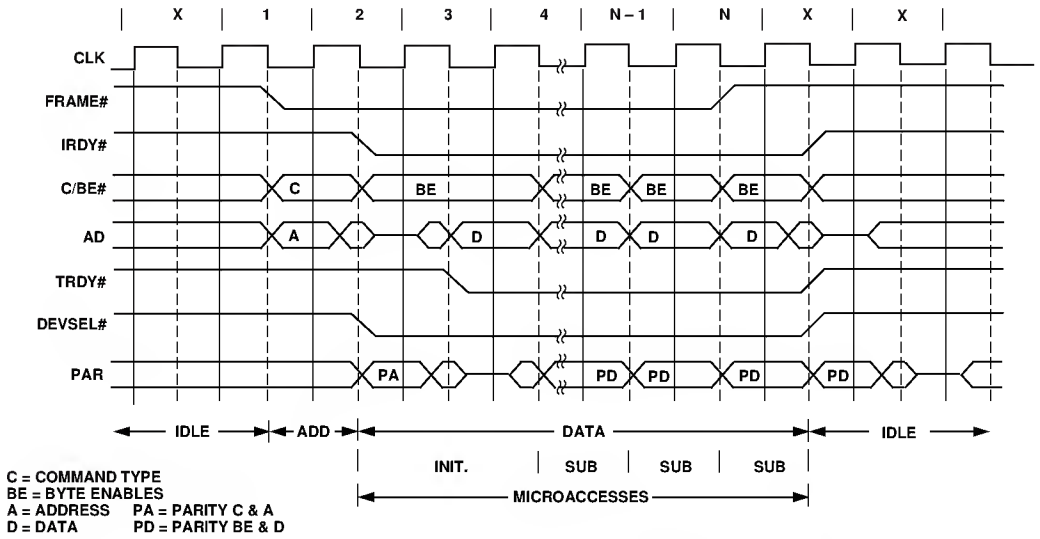


Figure 12. Master Burst Read Access Cycle

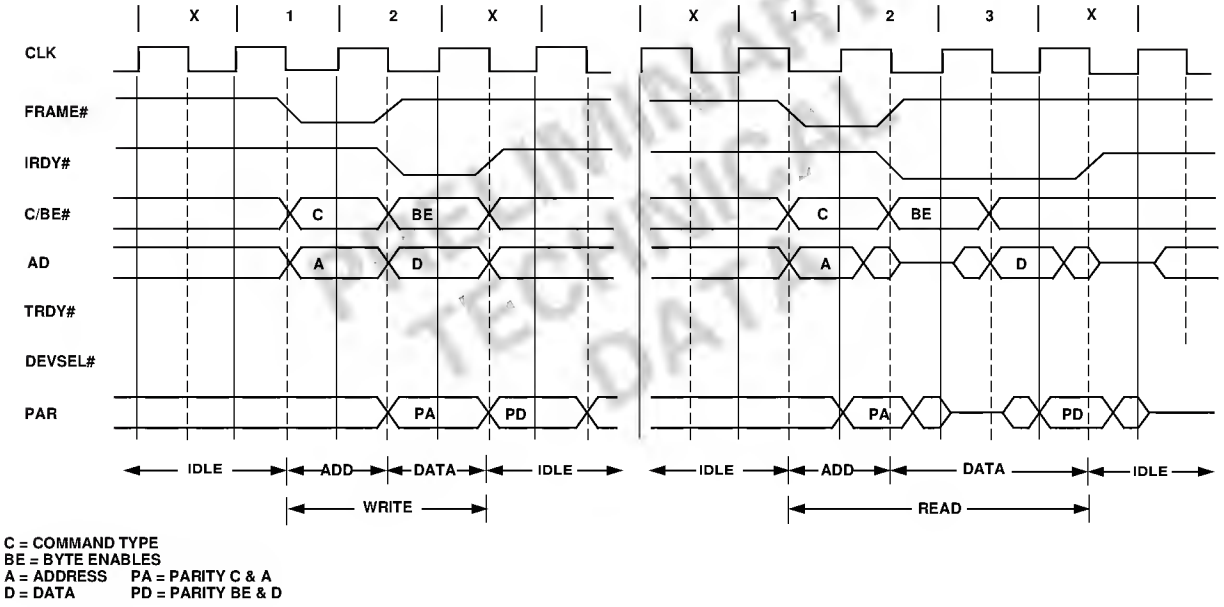


Figure 13. Master Single Write and Read Access Cycle

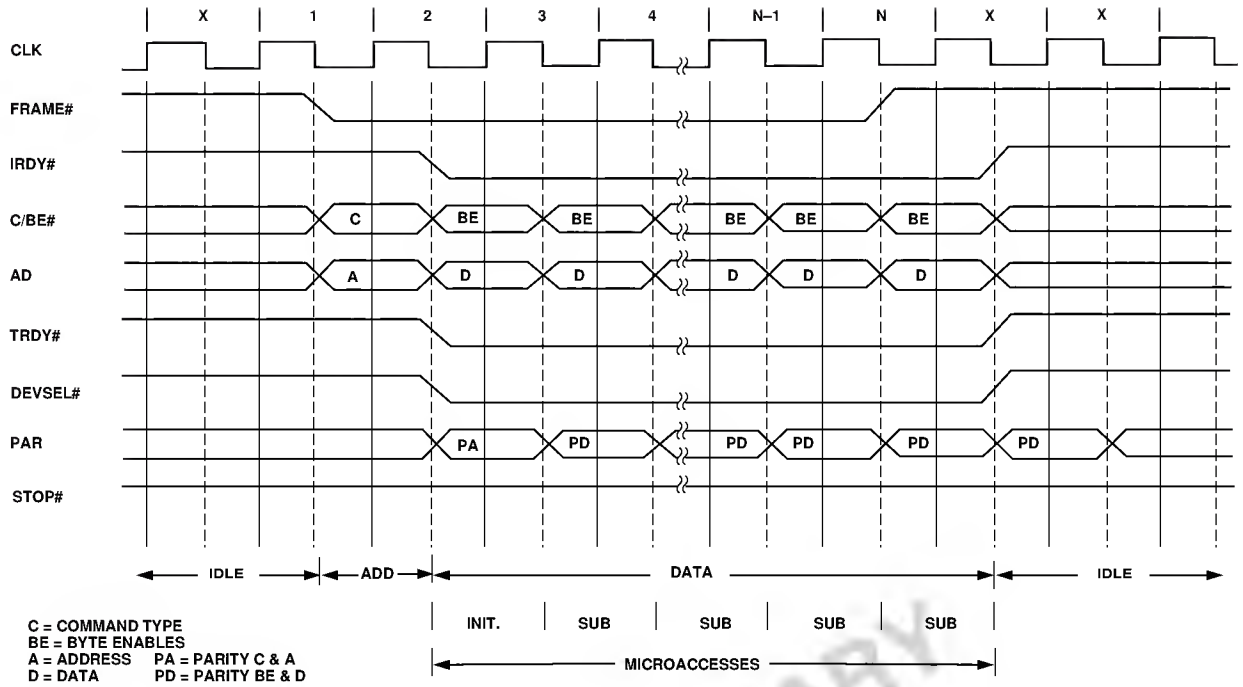


Figure 14. Master Burst Write Access Cycle

CLOCK SPECIFICATIONS*

	Min	Typ	Max	Units
Input Crystal/Clock Frequency		33		MHz
Input Clock Duty Cycle (When an External Clock Is Used Instead of a Crystal)	25/75		75/25	%
Initialization Sample Rate Change Time (Neglecting Pipeline Delay of 1/4 Sample Period)			0	ns

*Guaranteed, not tested.

PACKAGE CHARACTERISTICS

	Typ	Units
PQFP θ_{JA} (Thermal Resistance [Junction-to-Ambient])	TBD	°C/W
PQFP θ_{JC} (Thermal Resistance [Junction-to-Case])	TBD	°C/W

ABSOLUTE MAXIMUM RATINGS*

	Min	Typ	Max	Units
Power Supplies				
Digital (DV_{DD})	–0.3		6.0	V
Analog (AV_{DD})	–0.3		6.0	V
Input Current (Except Supply Pins)			±10.0	mA
Analog Input Voltage (Signal Pins)			AV_{DD} + 0.3	V
Digital Input Voltage (Signal Pins)			DV_{DD} + 0.3	V
Ambient Temperature (Operating)	0		+70	°C
Storage Temperature	–65		+150	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC SPECIFICATIONS FOR 5 V SIGNALING

Symbol	Parameter	Condition	Min	Max	Units	Notes
$I_{OH(AC)}$	Switching Current High (Test Point)	$0 < V_{OUT} \leq 1.4$ $1.4 < V_{OUT} < 2.4$ $3.1 < V_{OUT} < V_{CC}$ $V_{OUT} = 3.1$	–44 $-44 + (V_{OUT} - 1.4)/0.024$	 Equation A –142	mA mA mA	1 1, 2 1, 3 3
$I_{OL(AC)}$	Switching Current Low (Test Point)	$V_{OUT} \geq 2.2$ $2.2 > V_{OUT} > 0.55$ $0.71 > V_{OUT} > 0$ $V_{OUT} = 0.71$	95 $V_{OUT}/0.023$	 Equation B 206	mA mA mA	1 1 1, 3 3
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA	
$Slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V Load	1	5	V/ns	4
$Slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V Load	1	5	V/ns	4

NOTES

1. Refer to the V/I curves in Figure 4-3. Switching current characteristics for **REQ#** and **GNT#** are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to **CLK** and RST#, which are system outputs. "Switching Current High" specifications are not relevant to **SERR#**, **INTA#**, **INTB#**, **INTC#** and **INTD#**, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the ac drive point directly to the dc drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the first step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 4-3. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.

DC SPECIFICATIONS FOR 5 V SIGNALING

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{CC}	Supply Voltage		4.75	5.25	V	
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.5$	V	
V_{IL}	Input Low Voltage		–0.5	0.8	V	
I_{IH}	Input High Leakage Current	$V_{IN} = 2.7$		70	µA	1
I_{IL}	Input Low Leakage Current	$V_{IN} = 0.5$		–70	µA	1
V_{OH}	Output High Voltage	$I_{OUT} = -2$ mA	2.4		V	
V_{OL}	Output Low Voltage	$I_{OUT} = 3$ mA, 6 mA		0.55	V	2
C_{IN}	Input Pin Capacitance			10	pF	3
C_{CLK}	**CLK** Pin Capacitance		5	12	pF	
C_{IDSEL}	**IDSEL** Pin Capacitance			8	pF	4
L_{PIN}	Pin Inductance			20	nH	

NOTES

1. Input leakage currents include Hi-Z output leakage for all bidirectional buffers with three-state outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, **FRAME#**, **TRDY#**, **IRDY#**, **DEVSEL#**, **STOP#**, **SERR#**, **PERR#**, **LOCK#** and, when used, **AD[63::32]**, **C/BE[7::4]#**, **PAR64**, **REQ64#**, and **ACK64#**.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for **CLK**) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean, in general, that components for expansion boards would need to use alternatives to ceramic PGA packaging (i.e., PQFP, SGA, etc.).
4. Lower capacitance on this input only pin allows for nonresistive coupling to **AD[xx]**.

APPLICATION CIRCUITS

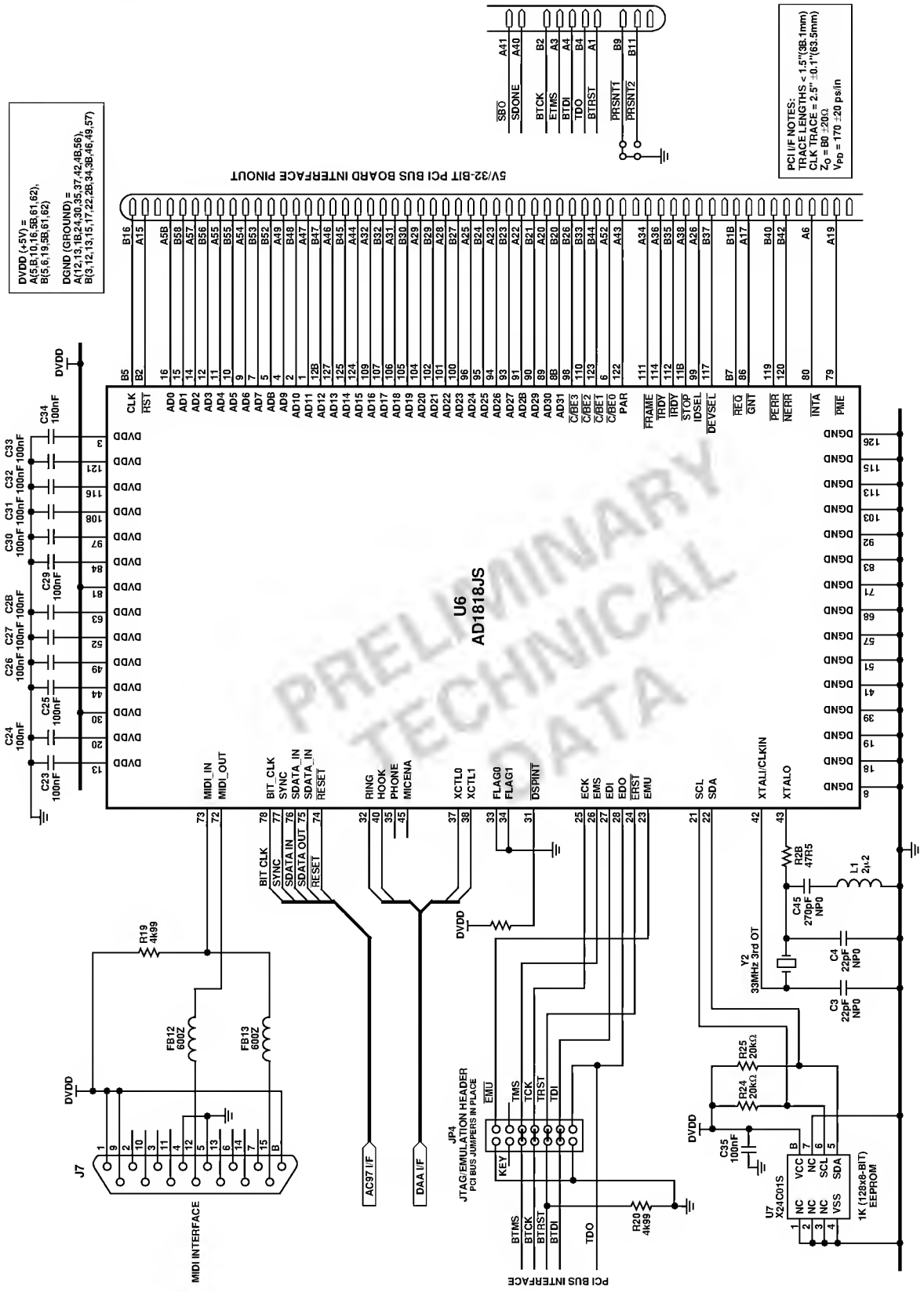


Figure 15.

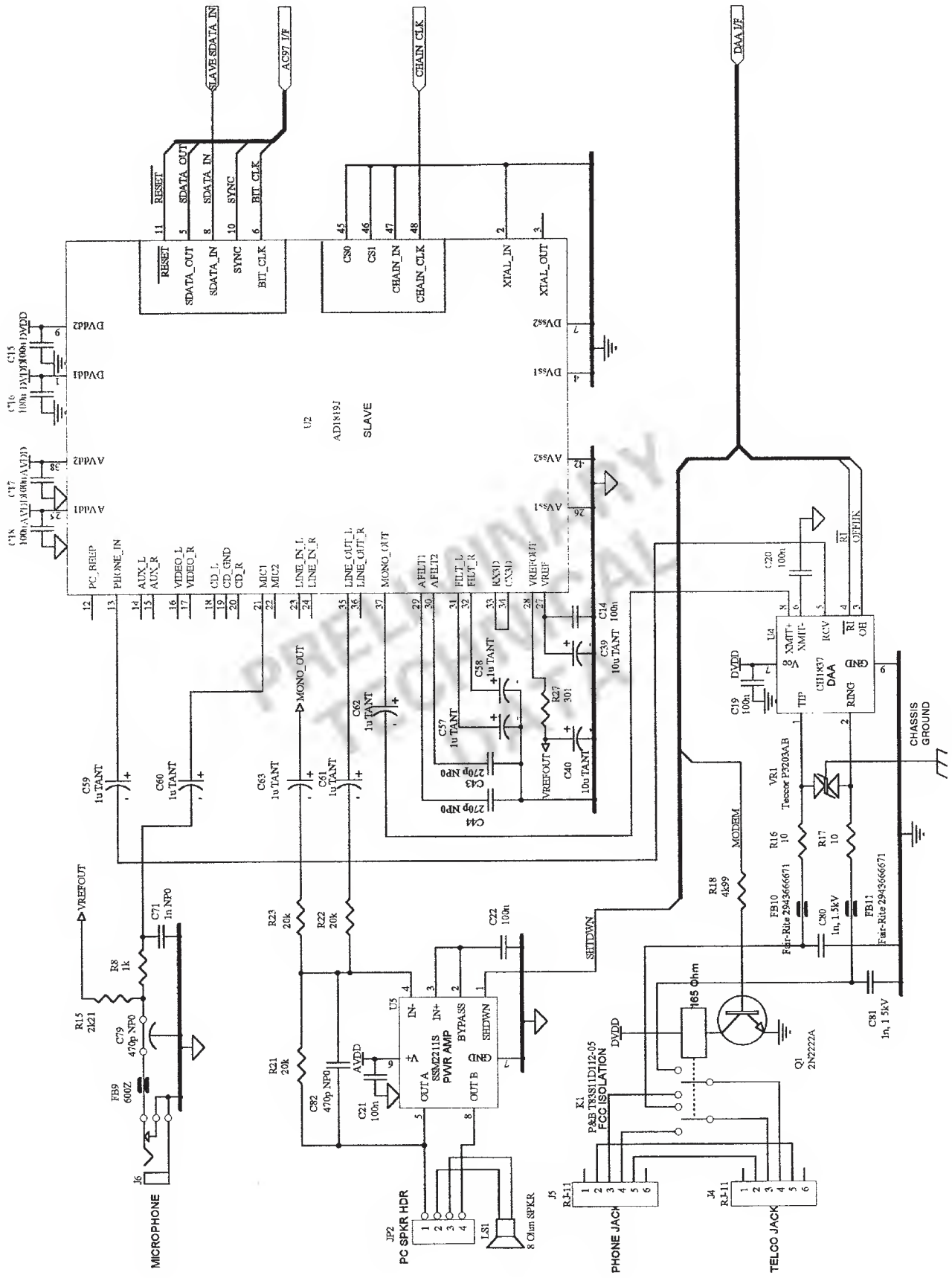

SLAVE SDATA IN
AC97 I/F
CHAIN CLK
DAA I/F
RESET
SDATA_OUT
SDATA_IN
SYNC
BIT_CLK
CS0
CS1
CHAIN_IN
CHAIN_CLK
XTAL_IN
XTAL_OUT
U2
AD1819J
SLAVE
DVDD
AVDD
PC_BEEP
PHONE_IN
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
LINE_OUT_L
LINE_OUT_R
MONO_OUT
AFILT1
AFILT2
FILT_L
FILT_R
RXN0
CXN0
VREFOUT
VREF
SHTDWN
MODEM
CHASSIS GROUND
MICROPHONE
PHONE JACK
TELCO JACK
PC SPKR HDR
8 Ohm SPKR
165 Ohm
P&B T83S11D112-05
FCC ISOLATION
SSM2211S
PWR AMP
Tecon P3203AB
CH1837
DAA
Fair-Rite 2943666671

Figure 16.

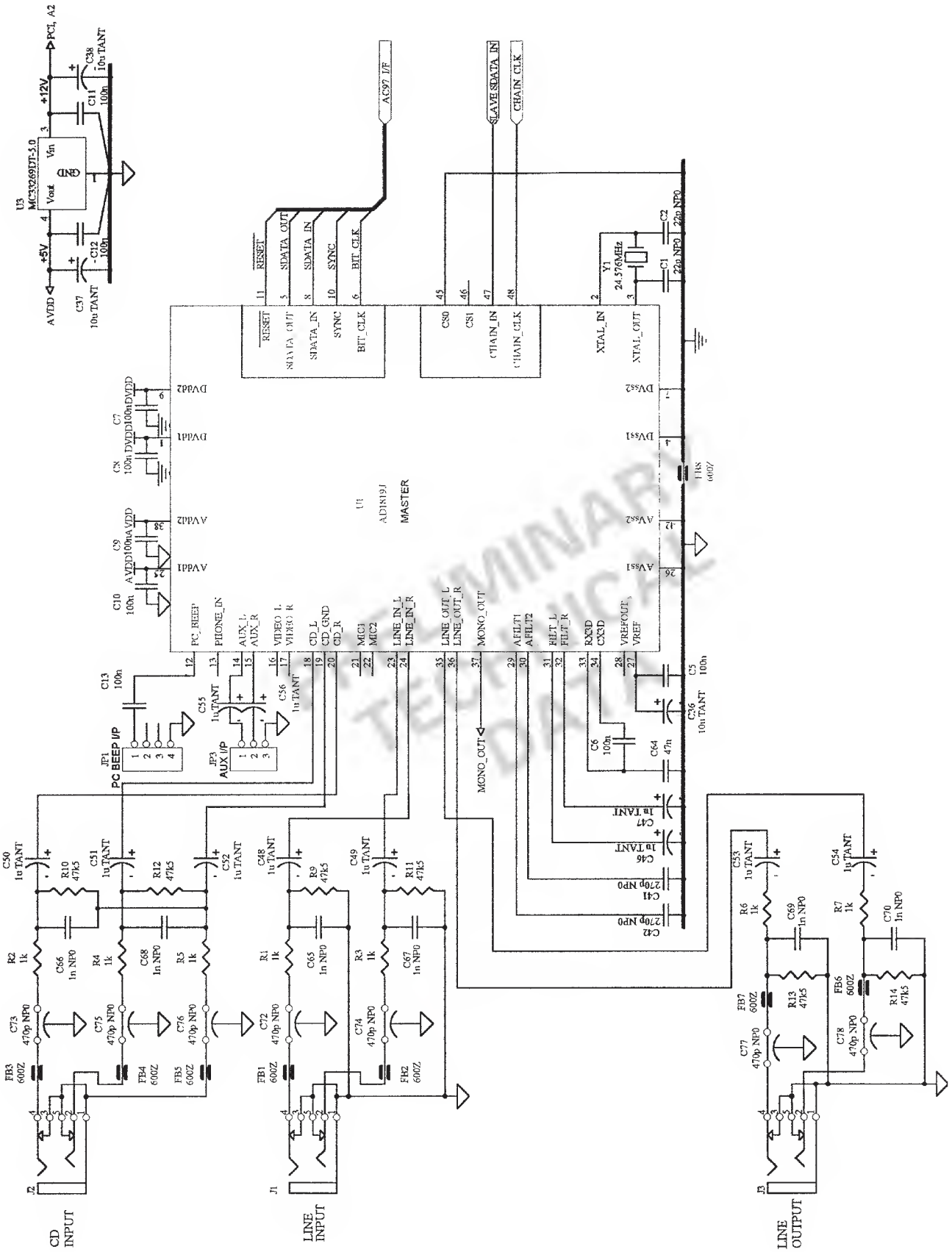

U1
AD1819J
MASTER
AC97 I/F
SLAVE SDATA_IN
CHAIN_CLK
PC1, A2
+12V
+5V
AVDD
U3
MC33269DT-3.0
C37 10u TANT
C38 10u TANT
C11 100n
C112 100n
Y1
24.576MHz
C1 22p NP0
C2 22p NP0
C5 100n
C36 10u TANT
C6 100n
C64 47n
C47 1u TANT
C46 1u TANT
C41 270p NP0
C42 270p NP0
C7 DVDD 100n
C8 100n
C9 AVDD 100n
C10 100n
C13 100n
C55 1u TANT
C56 1u TANT
JP1 PC BEEP I/P
JP3 AUX I/P
C50 1u TANT
C51 1u TANT
C52 1u TANT
C48 1u TANT
C49 1u TANT
C53 1u TANT
C54 1u TANT
R10 47k5
R12 47k5
R9 47k5
R11 47k5
R13 47k5
R14 47k5
R2 1k
R4 1k
R5 1k
R1 1k
R3 1k
R6 1k
R7 1k
C66 1n NP0
C68 1n NP0
C65 1n NP0
C67 1n NP0
C69 1n NP0
C70 1n NP0
C73 470p NP0
C75 470p NP0
C76 470p NP0
C72 470p NP0
C74 470p NP0
C77 470p NP0
C78 470p NP0
FB3 600Z
FB4 600Z
FB5 600Z
FB1 600Z
FB2 600Z
FB7 600Z
FB6 600Z
J2
J1
J3
CD INPUT
LINE INPUT
LINE OUTPUT
MONO_OUT
PRELIMINARY TECHNICAL DATA

Figure 17.

OUTLINE DIMENSIONS

Dimensions shown in mm and (inches).

128-Terminal Metric Plastic Quad Flatpack (PQFP)
(S-128A)